Common Management Interface Specification

Rev 4.0 May 8, 2019

Abstract: This document defines the Common Management Interface Specification (CMIS) that may be used by pluggable modules with host to module management communication based on a Two-Wire-Interface (TWI), such as QSFP Double Density (QSFP-DD), OSFP, COBO, QSFP, and SFP-DD. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules and transceivers.

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Foreword

The development work on this specification was done by the QSFP-DD, OSFP and COBO advisory group. Further revisions of the CMIS shall be backwards compatible to implementations conforming to Revision 4.0.

Revision History

Rev 3.0 August 17, 2018:

- Initial public release

Draft Rev 3.0.1 January 7, 2019:

- Converted InitMode signal to continuously-sampled LPMode
- Associated Module and Data Path State Machine changes
- Added LPMode Override bit
- Added pages 04h and 12h for tunable laser support
- Added diagnostic pages 13h and 14h
- New format to conform to SFF
- Added Command Data Block (CDB) section (pages 9Fh and A0h-AFh)

Draft Rev 4.0 May 8, 2019:

WARNING: Implementations compliant to CMIS Revision 4.0 of this specification will not interoperate with revision 3.0 implementations and vice-versa. The following specifications have changed:

- Converted InitMode signal to continuously-sampled LPMode
- Data Path initialization control (Page 10h) meaning/polarity has changed
- Added LowPwr register (Lower memory, Byte 26, bit 6) to switch power mode

Other changes:

- Added Scope statement
- Added Conventions
- Added Definitions
- Updated Introduction
- Consolidation of section 5
- Rework and Partial Consolidation of section 6
- Added Versatile Digital Diagnostics Monitoring (7.1)
- Added CDB Feature (7.2 and 9)
- Moved Examples to Appendix
- Change Upper Page Lower Page terminology (Upper and Lower Memory plus Pages)
- Removed Interface ID tables and replaced them with references to SFF-8024

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1 Scope and Purpose

This document defines the Common Management Interface Specification (CMIS) as a generic management interface together with a generic management interaction protocol between hosts and modules. The CMIS target audience therefore includes suppliers of modules and transceivers, system manufacturers, and system integrators.

CMIS has been developed to allow host and module software implementers to utilize a common code base across a variety of form factors. CMIS provides a set of core functionality that all modules must implement and a set of optional features whose implementation is advertised in the module memory map. This approach allows host software implementers to read and react to optional module capability advertisements while ensuring interoperability with all modules at a basic level.

Characteristic and common to all CMIS compliant modules is that management data is transferred over a Two-Wire-Interface (TWI), using a 256 byte addressable memory window, with mechanisms to dynamically page data of a much larger management memory space into the upper half of the host addressable memory window.

The *physical scope* of CMIS compliant pluggable modules includes form factors such as QSFP-DD, OSFP, or COBO. However, CMIS is a generic management interface specification and can be implemented in a variety of existing form factors, such as QSFP, or not yet designed form factors. Advertisement fields are provided in the memory map to identify the form factor.

The *functional scope* of CMIS compliant modules may range from electrical cable assemblies (hereafter also referred to as modules, unless cable assemblies are specifically mentioned) and active transceiver modules to versatile coherent DWDM modules with integrated framers. A possible classification distinguishes the following functional module types

(1) **data agnostic (basic) system interface modules** such as cable assemblies or active modules that map bit streams from host lanes to media lanes, e.g. SR-8 modules
(2) **data format aware (complex) system interface modules** that perform interface related data processing (such as lane deskewing and FEC codecs), e.g. 400ZR modules
(3) **data link terminals**, i.e. modules with internal framers for media side link termination, comprising framing, mapping, aggregation (multiplexing), switching, or distribution (inverse multiplex) functionality

The *specification scope* of this document release covers data agnostic interface modules with (multiples of) eight host electrical lanes and management communication based on a Two-Wire-Interface (TWI) bus as described on https://www.i2c-bus.org/twi-bus. The extensions for modules with more than 32 (4x8) lanes, for complex interface modules, or for link terminal modules is left to future revisions of this document, or to external extension specifications.

2 References and Conventions

2.1 Industry Documents

The following documents are relevant to this specification:

2.2 Sources

Copies of InfiniBand standards may be obtained from the InfiniBand Trade Association (IBTA) (http://www.infinibandta.org).

Copies of IEEE standards may be obtained from the Institute of Electrical and Electronics Engineers (IEEE) (https://www.ieee.org).

Copies of OIF Implementation Agreements may be obtained from the Optical Internetworking Forum (http://www.oiforum.com).

Copies of Common Language Equipment Identification specifications may be obtained from www.commonlanguage.com

2.3 Conventions

The following conventions are used throughout this document:

DEFINITIONS
Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the definitions or in the text where they first appear. The word or term may also be printed in **bold font**.

ORDER OF PRECEDENCE
If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and values.

LISTS
Lists sequenced by lowercase or uppercase letters show no ordering relationship between the listed items.

Lists sequenced by numbers show an ordering relationship between the listed items.

Lists are associated with an introductory paragraph or phrase, and are numbered relative to that paragraph or phrase (i.e., all lists begin with an a. or 1. entry).

NUMBERING CONVENTIONS
The ISO convention of decimal numbering is used (i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point). This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

Logical Operations
Logical operators are written in uppercase (OR, AND, NOT) and parentheses are used to clarify precedence.

Numerical Constants

Numerals without suffix are understood as numbers in decimal notation (e.g. 16)
Hexadecimal literals are marked with a suffix ‘h’ (e.g. 10h), often written with leading zeroes (0010h).
Binary literals are marked with a suffix ‘b’ (e.g. 10000b), often written with leading zeroes (00010000b)
The suffixes may be omitted for unambiguous cases like 0=0b=0h and 1=1b=1h.
Spaces may be inserted to make long hexadecimal or binary digit strings readable(0001 0000b).

Referencing Module Resources

In this specification, all references to lane numbers are based on the electrical connector interface lanes, unless otherwise indicated.
In cases where a status or control aspect is applicable only to lanes after multiplexing or demultiplexing has occurred, the status or control is intended to apply to all lanes in the data path, unless otherwise indicated.
All references to host lanes or media lanes in this document refer to the registers that control or describe those signals. When the term ‘lane’ is used without reference to ‘host’ or ‘media’, a host lane perspective is assumed.

Examples

Examples are printed in grey font for visual differentiation from specification text.

Auxiliary Test

Auxiliary text such as hints or notes are printed in *italic font* for visual differentiation from specification text.

Transition Signals (State Transition Conditions)

State transition conditions in state transition diagrams are also referred to as transition signals (symbolic names ending in S) in analogy to digital state machine circuit specifications.

3 Keywords, Acronyms, and Definitions

For the purposes of this document, the following keywords, acronyms, and definitions apply.

3.1 Keywords

May / may not: Indicates flexibility of choice with no implied preference.

Obsolete: Indicates that an item was defined in prior specifications but has been removed from this specification.

Optional: Describes features which are not required by the specification. However, if any feature defined by the specification is implemented, it shall be done in the same way as defined by the specification. Describing a feature as optional in the text is done to assist the reader.

Prohibited: Describes a feature, function, or coded value that is defined in a referenced specification to which this specification makes a reference, where the use of said feature, function, or coded value is not allowed for implementations of this specification.

Reserved: Defines the signal on a connector contact when its actual function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields, and code values; the bits, bytes, fields, and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

Restricted: Refers to features, bits, bytes, words, and fields that are set aside for other standardization purposes. If the context of the specification applies the restricted designation, then the restricted bit, byte, word, or field shall be treated as a reserved bit, byte, word, or field (e.g., a restricted byte uses the same value as defined for a reserved byte).

Shall: Indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this specification.

Should: Indicates flexibility of choice with a strongly preferred alternative.

Vendor specific: Indicates something (e.g., a bit, field, code value) that is not defined by this specification. Specification of the referenced item is determined by the manufacturer and may be used differently in various implementations.

3.2 Acronyms and Abbreviations

ACK: Acknowledge
ASCII: American Standard Code for Information Interchange (the numerical representation of a character)
BER: Bit Error Rate
CDB: Command Data Block
CDR: Clock and Data Recovery
CLEI: Common Language Equipment Identification
COR: Clear on read
VDM: Versatile Diagnostics Monitoring
DFB: Distributed Feedback Laser
DWDM: Dense Wavelength Division Multiplexing
EML: Externally Modulated Laser
EPL: Extended Payload Length
FEC: Forward Error Correction

FERC Frame Error Count
FP: Fabry-Perot Laser
LPL: Local Payload Length
MBR: Module Boot Record
NACK: Not Acknowledge
OUI: Organizationally Unique Identifier (A unique vendor code assigned by the IEEE)
RO: Read-Only
RW Readable and Writeable
SDA: bidirectional Serial Data
SCL: unidirectional Serial Clock
TEC: Thermoelectric Cooler
TWI: Two Wire Interface
VCSEL: Vertical Cavity Surface Emitting Laser
WDM: Wavelength Division Multiplexing
WR: Writeable

3.3 Definitions

Application: Where used as a defined term, Application is defined as a specific combination of an industry standard host electrical interface and an industry standard module media interface. See Section 6.2 for use.

Bank: A memory map architectural feature that enables multiple sets of memory map pages that have the same page numbers. See Section 8.1 for use.

Checksum: a number derived from a block of digital data for the purpose of detecting errors.

Custom: Custom fields and formats are defined by the module manufacturer and may be unique to a specific vendor.

Data Path: Host electrical and module media lanes grouped together into a logical concept. A data path represents a group of lanes that will be initialized, used and deinitialized together. A data path carries a multi-lane signal.

Flat Memory: Single 256-byte memory implemented without paging

Gray Coding: used with PAM4 modulation. Defines the mapping of 2 binary bits into 4 levels.
(0,0) maps to level 0
(0,1) maps to level 1
(1,1) maps to level 2
(1,0) maps to level 3

Host Interface: A host interface is defined as the high-speed electrical interface between the module and the host system. The requirements of a specific host interface are defined in the associated industry standard for that interface. See Section 6.1 for use.

Lane: A generic term for the elements associated with transport of one of the high speed signals in one of the module interfaces.

Lower Memory: The 128 bytes addressed by byte addresses 00h through 7fh.

Module: Pluggable transceivers and active or passive cable assembly terminations that plug into the host receptacle such as, but not limited to, those of QSFP-DD, OSFP, COBO, QSFP, and SFP-DD form factors - hereafter referred to as modules unless cable assemblies are specifically mentioned.

Media Interface: A media interface is defined as the high-speed interface between the module and the interconnect medium, such as wires or optical fibers. The requirements of a specific media interface are defined in the associated industry standard for that interface. See Section 6.1 for use.

NV: Non-Volatile memory: a type of memory that can retrieve stored information even after having been power cycled

OM2: cabled optical fiber containing 50/125 um multimode fiber with a minimum overfilled launch bandwidth of 500 MHz-km at 850 nm and 500 MHz-km at 1300 nm as IEC 60793-2-10 Type A1a.1 fiber.

OM3: cabled optical fiber containing 50/125 um laser optimized multimode fiber with a minimum overfilled launch bandwidth of 1500 MHz-km at 850 nm and 500 MHz-km at 1300 nm as well as an effective laser launch bandwidth of 2000 MHz-km at 850 nm in accordance with IEC 60793-2-10 Type A1a.2 fiber.

OM4: cabled optical fiber containing 50/125 um laser optimized multimode fiber with a minimum overfilled launch bandwidth of 3500 MHz-km at 850 nm and 500 MHz-km at 1300 nm as well as an effective laser launch bandwidth of 4700 MHz-km at 850 nm in accordance with IEC 60793-2-10 Type A1a.3 fiber.

OM5: cabled optical fiber containing 50/125 um laser optimized multimode fiber with a minimum overfilled launch bandwidth of 3500 MHz-km at 850 nm, 1850 MHz-km at 953 nm and 500 MHz-km at 1300 nm as well as an effective laser launch bandwidth of 4700 MHz-km at 850 nm and 2470 MHz-km at 953 nm in accordance with IEC 60793-2-10 Type A1a.4 fiber.

OMA: Optical Modulation Amplitude: The difference between two optical power levels, of a digital signal generated by an optical source, *e.g.,* a laser diode.

OSNR: Optical Signal to Noise Ratio: The ratio between the optical signal power in a given signal bandwidth and the noise power in a given noise reference bandwidth.

Page: A management memory segment of 128 bytes that can be mapped into Upper Memory.

Pave: Average Power: The average optical power

Port: A point of signal entry or signal exit at the module boundary.

Port Function: The functions and resources within the module that process an signal before leaving and after entering the module through a module port.

Post-cursor equalization: Rx output means used to reduce post-cursor ISI

Pre-cursor equalization: Rx output means used to reduce pre-cursor ISI

Pulse Amplitude Modulation, four levels (PAM4): a modulation scheme where two bits are mapped into four signal amplitude levels to enable transmission of two bits per symbol.

Rx: an electronic component (Rx) that converts an input signal (optical or electrical) to an electrical (retimed or non-retimed) output signal.

F16: a SFF-8636 Big Endian 16-bit data type representing an unsigned float value, with 5 bits for base-10 exponent, offset by -24, and 11 bits for mantissa. The format is: $m \cdot 10^{s+o}$ where m ranges from 0 to 2047, s ranges from 0 to 31 and o is fixed at -24. The smallest non-zero number is 1*10^(-24). The largest number supported is 2047*10^10. Within the 2 bytes of the value (stored lowest byte first), m and s are encoded as follows:

Byte	Bits	Description
1	7:3	Exponent (s)
1	2:0	Mantissa (m), bits 10:8
2	7:0	Mantissa (m), bits 7:0

SNR: Signal to Noise Ratio: The ratio of signal power to the noise power, expressed in decibels

tNACK: Time required for the module to accept a single or sequential write to volatile memory.

tWR: Time required to complete a single or sequential write to non-volatile memory.

Tx: a circuit (Tx) that converts an electrical input signal to a signal suitable for the communications media (optical or electrical).

Upper Memory: The 128 bytes addressed by byte addresses 80h through ffh.

4 Introduction and General Description

As a management interface specification CMIS defines the management interface and associated protocols for all required and allowable management interactions between a CMIS aware host and a CMIS compliant module that are relevant for the host using the module in an application.

4.1 CMIS Compliant Modules

CMIS Compliant Modules Symmetry is expected between the Tx and the Rx hardware structure; for example Tx lanes that are multiplexed in the Tx are demultiplexed in the Rx. Each Application selected by the host is applied to the same Tx and Rx host electrical lanes.

4.2 Management Protocol Layers

The management interface is best understood in terms of its protocol layers:

• The physical interconnection layer is the lowest layer comprising the electrical and mechanical interface elements (that are required to carry elementary signals) as well as the associated protocols for using those elements. Since CMIS is targeted to multiple form factors, the physical layer is defined in the relevant module form factor specification. In CMIS generic names are used instead of form-factor specific names. Refer to Appendix A Form Factor Specific Signal Names for the association between generic management signal names used herein and the form-factor specific signal names.

• The basic management data transfer layer provides the protocols required to let the host and the module exchange elementary management operations (and associated data) via the physical interconnection layer. The basic management operations in CMIS are reading and writing bytes from or to a 256-byte addressable memory window. The mechanisms and protocols pertinent to this layer are defined in section 5. Extensions required to effectively address a larger management memory space are described in section 8.

• An optional management message exchange layer can be implemented on top of the basic management data transfer layer and provides primitives for management message exchange between host and module. This layer is described in sections 7.2 and 9.

• The management application layer specifies the effects of management operations, be it memory registers or messages exchanged, on function or behavior of the module as well as any associated behavioral protocols. This layer is described in sections 6 and 8.

5 Management Interface

The physical layer of the management interface between host and module consists of a serial communication interface and a small set of discrete hardware signals.

5.1 Management Control Signals

The following discrete hardware signals are required by CMIS

- a signal allowing the host to request a module reset (**ResetL**)
- a signal allowing the host to control full or partial power up of the module (**LPMode**)
- a signal allowing the module to assert an interrupt request (**Interrupt**) to the host

These generic control signals are mapped to form factor dependent signals in Appendix A

5.2 Management Communication Interface

5.2.1 General Description

The management communication interface provides a number of elementary management operations that allow the host to read from or write to byte-sized management registers in the management memory map of the module. There are read and write operations both for single bytes and for contiguous byte sequences. Two types of read operations, either with implicit addressing (read from current address) or with explicit addressing, are supported.

The management communication interface distinguishes a **master** role and a **slave** role. The host shall be the master and the module shall be the slave.

The master initiates all operations that lead to data transfer. Data can be transferred from the master to the slave (in write operations) and from the slave to the master (in read operations).

The management communication interface is assumed to be a point-to-point connection.

Note: In order to allow access to multiple modules on a shared management communication bus, some form factors include and require the module to support a module select signal, (ModSelL). For these form factors, before initiating a management communication, the host shall provide setup time on the ModSelL line of all modules on the same bus. The host shall not change the ModSelL line of any module until the management communication is complete and a hold time requirement is satisfied.

5.2.2 Physical Layer

The physical layer supporting communication between host and module is the Two Wire serial Interface (**TWI**). The TWI consists of a clock signal (**SCL**) and a data signal (**SDA**).

The master drives the SCL signal to clock data and control information onto the TWI bus. Both master and slave shall latch the state of SDA on the positive transitioning edge of SCL. The host shall initially use a 0-400 kHz SCL clock speed. If a higher management interface speed is supported by the module (see appropriate Hardware Specification) the host may later switch to the faster 0-1 MHz SCL clock speed.

The SDA signal is bi-directional. During binary data transfer, the SDA signal shall transition when SCL is low. SDA transitions when SCL is high are used to mark either the beginning (**START**) or ending (**STOP**) of a data transfer.

Both control bytes and data bytes are transferred bit-serially over the SDA. A LOW voltage encodes 0. A HIGH voltage encodes 1.

The associated protocol to implement the elementary management operation (as byte transfers) over the TWI bit-serial communication link is described in detail in the remainder of this section.

Electrical specifications and TWI timing specifications are found in the appropriate hardware/module specification.

5.3 Serial Communication Protocol

A serial communication protocol over the TWI bus is used to implement management register access operations.

5.3.1 Basic Definitions

5.3.1.1 Start Condition (START)

A high-to-low transition of SDA with SCL high is a START condition.

All TWI bus operations begin with a START condition generated by the master.

5.3.1.2 Stop Condition (STOP)

A low-to-high transition of SDA with SCL high is a STOP condition.

All regular TWI bus operations end with a STOP condition generated by the master.

5.3.1.3 Word Size (Byte)

The TWI word size is 8-bits. TWI words are transferred bit-serially with the most significant bit (MSB) first.

Note: The following text uses the term byte to refer to 8-bit words.

5.3.1.4 Basic Operation Encoding (Control Byte)

The generic TWI address byte is also used to carry a control bit indicating the type of basic management operation. TWI address 10100001b (A1h) indicates a read operation. TWI address 10100000b (A0h) indicates a write operation.

In this specification, the TWI address values 10100001b (A1h) and 10100000b (A0h) are also referred to as a write control byte and read control byte, respectively.

5.3.1.5 Acknowledge (ACK)

After sending a byte, the side driving the TWI bus releases the SDA line for one bit time. During this period the receiving side of the TWI bus pulls SDA low (zero) in order to acknowledge (**ACK**) that it has received the byte.

Not pulling the SDA low in this period is interpreted as a negative acknowledge (**NACK**).

The slave shall ACK each individual control byte received during a read or write operation, and it shall ACK each individual data byte received during a write operation.

The master shall ACK each individual data byte received during a read operation, except for the last data byte, where it terminates the read operation by sending a NACK and STOP.

5.3.1.6 Clock Stretching

To extend the TWI data transfer the slave may pull the clock SCL low. This pull down shall be initiated only while SCL is low. This mechanism can be used by the slave to delay completion of the current basic operation.

5.3.1.7 Acknowledge Polling

After a properly terminated write operation, the slave is allowed to disable its inputs in order to internally realize and finalize the write operation.

Apart from specified maximum durations, the master does not know when exactly the slave is ready to accept the next basic management operation. In this situation the master can use the following acknowledge polling procedure to initiate the next basic management operation as soon as the slave is ready to accept it:

When the slave does not ACK the first byte of an operation (the device address), the master can just repeat sending the START condition followed by the first byte of the operation, until the slave eventually ACKs the first byte.

5.3.2 Protocol Reset and Recovery

5.3.2.1 Power On Reset

The interface shall enter a reset state upon application of power.

5.3.2.2 Protocol Reset and Recovery

Synchronization issues may cause the master and slave to disagree on the specific bit location currently being transferred, the type of operation or even if an operation is in progress. The TWI protocol has no explicitly defined reset mechanism. The following procedure may force completion of the current operation and cause the slave to release SDA.

1. The master shall provide up to a maximum of nine SCL clock cycles (drive low, then high) to the slave
2. The master shall monitor SDA while SCL is high on each cycle.
3. On any clock cycle, if the slave releases SDA, the master shall initiate a STOP condition. The master is then free to send a START condition for the next operation
4. If SDA remains low after nine clock cycles the TWI protocol reset has failed

5.3.3 Binary Serial Frame Format for Basic Operations

5.3.3.1 Read/Write Control Byte and Response

After the START condition, the first byte of a TWI bus operation is a control byte consisting of a fixed 7-bit part 1010000b followed by a bit indicating the type of operation: A read operation is requested if this bit is 1 (high). A write operation is requested if this bit is 0 (low).

Upon reception of the control byte the slave asserts the SDA signal low to acknowledge (ACK) receipt.

5.3.3.2 Byte Address and Data

Following the control byte, addresses and/or data are transmitted in units of bytes.

In sequential read or write operations (i.e. when transferring multiple data bytes in one operation) the data bytes are transmitted in increasing byte address order over the TWI.

5.4 Read/Write Operations

5.4.1 Slave Memory Current Byte Address Counter (Read and Write Operations)

The slave maintains an internal current byte address counter containing the byte address accessed during the latest read or write operation incremented by one with roll-over as follows: The current byte address counter rolls-over after a read or write operation at the last byte address of the current 128-byte memory page (127 or 255) to the first byte address (0 or 128) of the same 128-byte memory page.

The current byte address counter is incremented whenever a data byte is received or sent by the slave as part of properly terminated management operation.

Note: The current byte address counter rollover behavior may be different in certain (optional) address ranges, such as the optional CDB message exchange mechanism described in section 7.2

There is only one current byte address counter and it will change on every TWI transaction. The current byte address counter remains valid between operations as long as power to the slave is maintained and as long as no protocol violations occur. Upon loss of power to or reset of the module or upon operations not terminated by a Stop condition, the current byte address counter contents may be indeterminate.

5.4.2 Data Coherency

Data coherency for two-byte entities in the module management memory map) can be achieved as follows: The master shall use (sequences of) 2-byte sequential reads (see subsection 5.4.4) to retrieve 2-byte data. The slave shall prevent that the master acquires partially updated 2-byte data during any individual 2-byte sequential read.

Data consistency for accesses to more than two bytes requires a application level interaction protocols using fields in the register map. It is not guaranteed by the basic TWI R/W operations.

Note: An example of such a protocol is the CDB message exchange mechanism described in section 7.2

5.4.3 Byte Read Operations

5.4.3.1 Current Address Read Operation

The master begins the current address read operation with START and then sends the read control byte (10100001).

The slave sends ACK followed by the byte stored at the address given by the current byte address counter.

The master terminates the operation with NACK and STOP.

The slave increments its current byte address counter after orderly termination of the operation.

		<--- CONTROL BYTE --->																		
MASTER	START	MSB						LSB	READ									NACK	STOP
		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
SLAVE										ACK	MSB							LSB		
											<---- DATA BYTE ----->									

Figure 5-1 Module Current Address Read Operation

5.4.3.2 Random Read Operation

A random read operation is implemented as a dummy write operation, followed by a current address read operation.

The dummy write operation is used to load the target byte address into the current byte address counter, from which the subsequent current address read operation then reads. The procedure is as follows:

The master generates a START condition and sends the target byte address after the write control byte (10100000b). The master then generates another START condition (aborting the dummy write) and begins a current address read operation by sending a read control byte (10100001b).

The slave acknowledges each byte received. When the byte address of the dummy write is received, the slave updates the current byte address counter. Since the slave then sees the write operation aborted (i.e. when it receives a START instead of a byte to be written), the current byte address counter is not incremented and so contains the address to be read in the subsequent current address read operation.

The master terminates the operation with NACK and STOP when it has received the requested byte.

The slave increments its current byte address counter after orderly termination of the operation and before accepting a new basic management operation.

		<--CONTROL BYTE -->									<BYTE ADDRESS>								
MASTER	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0
SLAVE										ACK									ACK

	<- CONTROL BYTE -->																		
START	MSB						LSB	READ										NACK	STOP
	1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
									ACK	MSB							LSB		
										<---- DATA BYTE n---->									

Figure 5-2 Module Random Read

5.4.4 Sequential Bytes Read Operation

A sequential read operation is the continuation either of a current address read (see Figure 5-3) or of a random address read (see Figure 5-4).

The master indicates continuation of a reading sequence (i.e. sequential read operation) to the slave by sending an ACK after a data byte received (instead of terminating the operation with NACK and STOP).

When the slave receives an ACK after sending a byte to the master, it increments the current byte address counter and sends the byte that is stored at this address.

The sequential read is terminated when the master sends a NACK and a STOP (instead of an acknowledge ACK).

The slave increments its current byte address counter after orderly termination of the operation and before accepting a new basic management operation.

5.4.4.1 Sequential Read from Current Start Address

		<- CONTROL BYTE -->																
MASTER	START	MSB						LSB	READ									ACK
		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	0
SLAVE										ACK	MSB							LSB	
											<---- DATA BYTE n---->								

								ACK									NACK	STOP
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1	
MSB							LSB		MSB							LSB		
<-- DATA BYTE n+1 --->									<-- DATA BYTE n+x --->									

Figure 5-3 Sequential Address Read Starting at Module Current Address

5.4.4.2 Sequential Read from Random Start Address

		<- CONTROL BYTE -->									<BYTE ADDRESS>								
MASTER	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0
SLAVE										ACK									ACK

	<- CONTROL BYTE -->																	
START	MSB						LSB	READ										ACK
	1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	0
									ACK	MSB							LSB	
										<---- DATA BYTE n---->								

								ACK									NACK	STOP
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1	
MSB							LSB		MSB							LSB		
<-- DATA BYTE n+1 --->									<-- DATA BYTE n+x --->									

Figure 5-4 Sequential Address Read Starting with Random Module Read

5.4.5 Byte Write Operation

The master generates a START condition and sends the write control byte (10100000b). When the slave has responded to the write control byte with ACK, the master sends the target byte address. When the slave has responded to the target byte address with ACK, the master sends the data byte value. When the slave has responded to the data byte value with ACK, the master sends STOP to terminate the write operation. Otherwise the write operation is aborted.

On receipt of the target byte address, the slave immediately updates its current byte address counter. However, the slave begins its internal write cycle of the received data byte to the address in the byte address counter not before the write operation is properly terminated by STOP. The slave eventually increments the current byte address counter before accepting then next basic management operation.

If a START condition is received in place of a STOP condition the slave discards the data byte received and does not increment the current byte address counter.

For writes to non-volatile memory, upon receipt of the proper STOP condition, the slave may enter an internally timed write cycle, with maximum duration tWR, to internal memory. For writes to volatile memory the slave may enter an internally timed write cycle, with maximum duration tNACK, to internal memory.

Note: See the appropriate Hardware specification for tWR and tNACK timing specifications.

The slave may disable its management interface input during an internally timed write cycle and not respond or acknowledge subsequent commands until the internal memory write cycle is complete.

Note: the TWI 'Combined Format' using repeated START conditions is not supported on write commands.

		<- CONTROL BYTE -->									<BYTE ADDRESS>									<- DATA BYTE ->									
MASTER	START	MSB						LSB	WRITE		MSB							LSB		MSB							LSB		STOP
		1	0	1	0	0	0	0	0	0	x	x	x	X	x	x	x	x	0	x	x	x	x	x	x	x	x	0	
SLAVE										ACK									ACK									ACK	

Figure 5-5 Module Write Byte Operation

5.4.6 Sequential Bytes Write Operation

The master initiates a sequential write operation of up to eight bytes in the same way as a single byte write, but it then does not send a STOP condition after the first byte. Instead, after the slave acknowledges (ACK) receipt of the first data byte, the master transmits up to seven additional data bytes without transmitting new explicit byte address information or control bytes.

Note: For transfers of data blocks larger than eight bytes see section 7.2.

The master terminates the sequential write sequence with a STOP condition, otherwise, the operation is aborted and the results of the sequential write are undetermined.

The master shall not include a mixture of volatile and non-volatile registers in the same sequential write.

The slave shall ACK each byte received. The slave may either store a data byte after sending ACK or it may decide to buffer all bytes of the sequential write operation until the operation is terminated by STOP.

After a properly terminated sequential write operation (STOP received) the slave ensures that the current byte address counter contains the address of the next byte after the last byte written, before accepting then next basic management operation. Otherwise, the value of the current byte address counter is undetermined.

Note: At the end of each 128 byte page, the current byte address counter rolls over to the first byte of that page.

For writes to non-volatile memory, upon receipt of the proper STOP condition the slave may enter an internally timed write cycle, with maximum duration tWR, to internal memory. For writes to volatile memory the slave may enter an internally timed write cycle, with maximum duration tNACK, to internal memory.

Note: See the appropriate Hardware specification for tWR and tNACK timing specifications.

The slave may disable its management interface input during an internally timed write cycle and not respond or acknowledge subsequent commands until the internal memory write is complete.

Note that TWI 'combined format' using repeated START conditions is not supported on sequential write commands.

		<- CONTROL BYTE -->									<BYTE OFFSET ADDRESS>								
MASTER	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0
SLAVE										ACK									ACK

MSB							LSB		MSB							LSB			
x	x	x	x	x	x	x	x	0	x	x	x	x	X	x	x	x	0		
								ACK									ACK		
<--- DATA BYTE n --->									<--- DATA BYTE n+1--->										

MSB							LSB		MSB							LSB				STOP
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0			
								ACK									ACK			
<--- DATA BYTE n+2--->									<--- DATA BYTE n+x--->											

Figure 5-6 Module Sequential Write Operation

5.5 Timing Specifications

Timing specifications for TWI operations are found in the appropriate hardware/module specification.

Timing specifications for module functions such as module soft control, status, squelch and disable can be found in the appropriate Module Hardware Specification, or they are either specified or advertised in this document.

6 Core Management Features

The behaviors described in this section are required for all CMIS modules, unless otherwise noted.

6.1 Module Management Basics

Typical CMIS modules have two interfaces between module internal circuitry and external connectors and systems – a host interface and a media interface.

6.1.1 Host Interface Conventions

The host interface is defined as the high-speed electrical interface between the module and the electrical connector in the host system. The host interface consists of signals that travel from the host into the module, referred to as transmitter input signals, and signals that travel from the module into the host, referred to as receiver output signals. All host interface signals are carried between the host and module over electrical differential pairs called host lanes.

6.1.2 Media Interface Conventions

The media interface is defined as the high-speed interface between the module and the interconnect medium, such as wires or optical fibers. The media interface consists of signals that travel from the module into the media, referred to as transmitter output signals, and signals that travel from the media into the module, referred to as receiver input signals. Each unique media interface signal, whether conveyed over a differential pair of electrical wires or an optical wavelength on a physical fiber, is called a media lane.

6.1.3 Interface Memory Map Representations

A set of registers is associated with each interface to control and report status for signals at that interface. All references to host lanes or media lanes in this document refer to the respective registers that control or describe those signals. When the term ‘lane’ is used without reference to ‘host’ or ‘media’ in this specification, a host lane perspective is assumed.

In many cases, module resources are associated with host interface lanes or media interface lanes as a specification convenience, even though the resource may not be physically proximate to the associated interface.

6.2 Module Functional Model

The following sections define functional aspects common to all CMIS modules, unless otherwise noted.

6.2.1 Functional Module Capabilities – Applications

The module uses Applications to advertise the set of industry standards that it supports. An Application is defined as a combination of an industry standard host interface and an industry standard media interface. These standards define all necessary attributes for the respective interface, including the signaling baud rate, the signaling modulation format and the number of lanes. A module may support multiple different Applications and/or multiple instances of the same Application.

An Application consists of one or more host electrical lanes and one or more module media lanes. The module advertises the lane or group of lanes onto which an instance of an Application can be assigned. The lane or group of lanes supported by the instance of the Application are identified by the lowest numbered lane in that instance. This identification is advertised for both the host electrical and module media interfaces. Within each instance of an Application, all lanes shall be numbered consecutively on both interfaces, starting with the advertised lowest lane number.

A module may advertise support for a single Application. For example, a module advertises an Application that consists of a CAUI-4 host electrical interface and a 100GBASE-SR4 media interface combination. In this example, the module could advertise support for one or two instances of the Application. Each instance of the Application selected by the host is independent of other Application instances.

A module may also advertise support for multiple Applications. For example, a module advertises an Application that consists of a 400GAUI-8 host electrical interface and a 400GBASE-DR4 media interface combination, and a second Application that consists of a 100GAUI-2 host electrical interface and a 100GBASE-DR media interface combination. The host may select one instance of the first Application or up to four instances of the second Application. Each instance of each selected Application is independent of other Application instances.

For each Application where the module supports multiple Application instances, hosts need to be able to determine which host electrical lane group corresponds to which module media lane group for each possible Application instance in the module. Modules shall associate the Nth host electrical lane group of the Application with the Nth module media lane group for the same Application. This rule is best illustrated by means of an example. A module advertising support for four instances of a 100GAUI-2 to 100GBASE-DR Application must identify the lowest lane number for each instance on both interfaces. As shown in Figure 6-1 for this example, the Application can be assigned starting on host electrical lane 1, 3, 5, or 7. These possibilities are the first, second, third, and fourth lane groups. By rule, the first lane group on the media interface in this example, which starts at media lane 1, must correspond to the first lane group on the host interface, which starts on host lane 1. The second lane group on the media interface, which starts on media lane 2, must correspond to the second lane group on the host interface, which starts on host lane 3, and so on. Therefore, in this example, the module would advertise host electrical lanes 1, 3, 5, and 7 are supported as the lowest numbered host lane for each instance of the Application, and module media lanes 1, 2, 3, and 4 are supported as the corresponding lowest numbered media lanes.

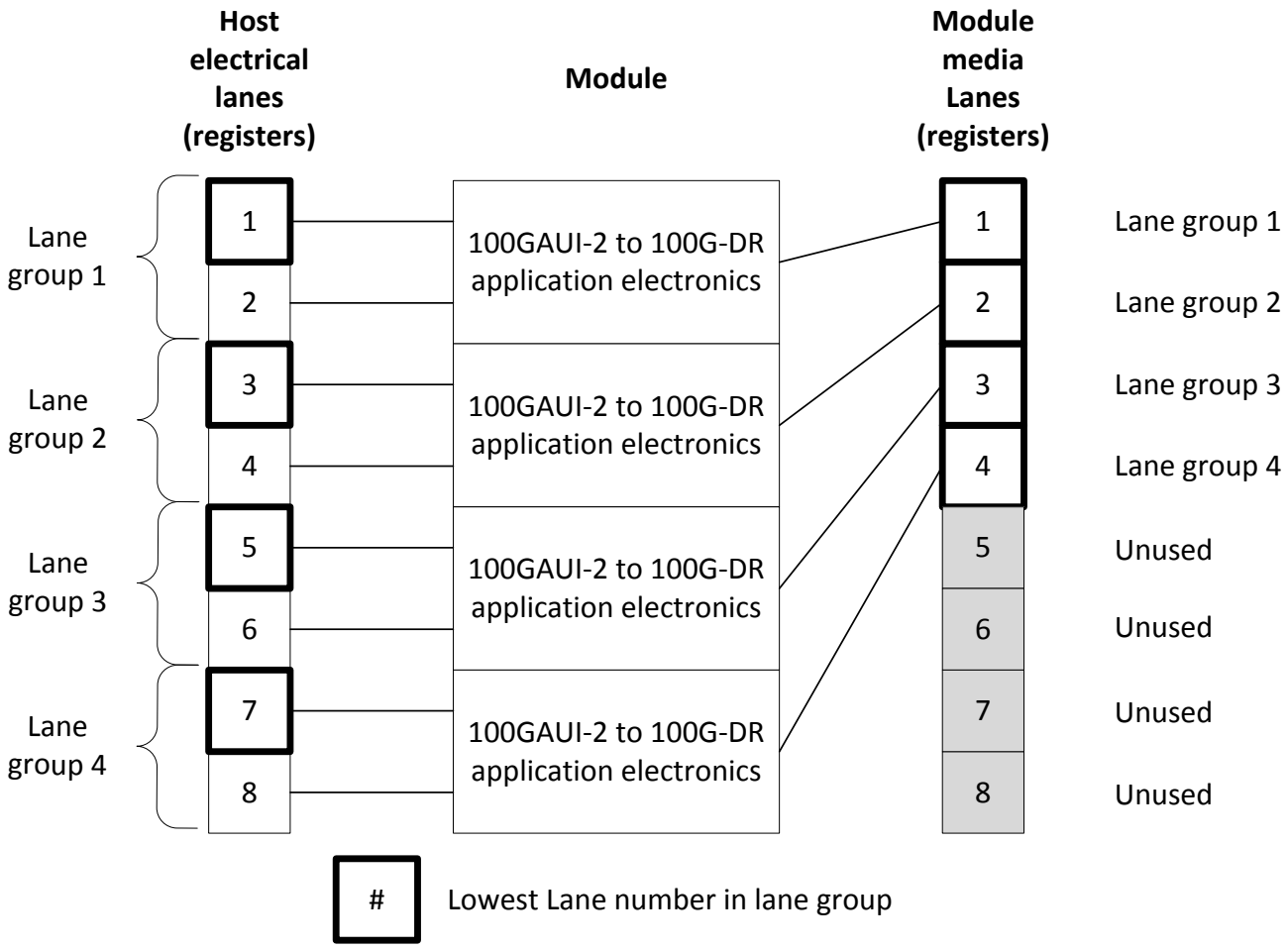


Figure 6-1 Lane Assignment Example

6.2.1.1 Advertising Methodology

The module identifies supported Applications through a set of Application Advertising registers. Within the Application Advertising areas of the memory map, each Application is described by a group of registers, shown in Table 6-1. This specification assigns a unique Application Select code (ApSel code) to each of these register groups. The host uses the ApSel code to select the advertised Application.

In the first byte, the Host Electrical Interface ID identifies the industry standard for the host electrical interface. The list of defined IDs can be found in SFF-8024 where each Host Interface ID is associated with an industry standard, host interface signaling rate, modulation format, and lane count(s). The module defines the maximum supported host interface lane count in the Host Lane Count field, described below. The first unused entry in the table shall be coded FFh to indicate the end of the list of supported Applications.

In the second byte, the Module Media Interface ID identifies the industry standard for the Module Media interface. The list of defined IDs can be found in SFF-8024 Interfaces and Associated IDs in one of the media interface tables. The module identifies which module media interface table applies to the module using the Module Type advertising field in Lower Page 00h Byte 85. The module media interface tables identify the media interface signaling rate, modulation format, and standard-defined lane count(s) for each Module Media Interface ID. The module defines the maximum supported media interface lane count in the Media Lane Count field, described below.

The third byte defines the number of lanes for the host electrical interface and the module media interface. The lane counts shall be consistent with the standards identified in the first and second bytes.

The fourth and fifth bytes identify the lanes where the Application is supported on the host and media interfaces, respectively. The module may support multiple instances of a given Application, so each Lane Assignment Options field identifies the lowest numbered lane in a consecutive group of lanes to which the Application can be assigned. For example, a module supporting two instances of an Application with a CAUI-4 host interface that can be assigned to Host electrical interface lanes 1-4 and 5-8 would advertise a Host Lane Assignment Options value of 00010001b, to indicate that the lowest numbered lane for assignment of an instance of the Application can be lane 1 or lane 5. The fifth byte (Media Lane Assignment Options) identifies where the Application instance is supported on the media interface. The Media Lane Assignment Options register is located on memory map page 01h in Table 8-38, separate from the first four bytes. The Media Lane Assignment Options register is not required for flat memory map modules.

Table 6-1 Module Application Advertising format for one application

Byte	Bits	Name	Description
First	7-0	Host Electrical Interface ID	ID from SFF-8024. The first unused entry in the table shall be coded FFh to indicate the end of the list of supported Applications.
Second	7-0	Module Media Interface ID	ID from SFF-8024. The table to use is identified by the Module Type Encoding in Table 8-12
Third	7-4	Host Lane Count	Number of host electrical lanes 0000b=lane count defined by interface ID (see SFF-8024) 0001b=1 lane, 0010b=2 lanes...1000b=8 lanes 1001b-1111b=reserved
	3-0	Media Lane Count	Number of module media lanes. For cable assemblies, this is the number of lanes in the cable. 0000b=lane count defined by interface ID (see SFF-8024) 0001b=1 lane, 0010b=2 lanes...1000b=8 lanes 1001b-1111b=reserved
Fourth	7-0	Host Lane Assignment Options	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit value of 1b indicates that the Application is allowed to begin on the corresponding host lane. In multi-lane Applications each Application shall use contiguous host lane numbers. If multiple instances of a single Application are allowed each starting point is identified. If multiple instances are advertised, all instance must be supported concurrently.
Fifth	7-0	Media Lane Assignment Options	Bits 0-7 form a bit map and correspond to Media Lanes 1-8. A bit value 1b indicates that the Application is allowed to begin on the corresponding media lane. In multi-lane Applications each Application shall use contiguous media lane numbers. If multiple instances of a single Application are allowed each supported starting point is identified. If multiple instances are advertised, all instances must be supported concurrently. This field is not required for flat memory map modules.

This specification provides space for advertisement of up to fifteen Applications. All modules advertise one or more Applications. The module shall advertise the Application used as the power up default in ApSel code 1. The Module Media Interface ID associated with ApSel 1 identifies the common name for the module. The module shall advertise its alternate Applications sequentially starting from ApSel code 2. ApSel codes 1-8 are advertised using Table 8-13, and ApSel codes 9-15 are advertised using Table 8-39.

Notes:

a. The advertised Application describes the host-media interface combination. It is the module's responsibility to advertise only valid combinations. Hosts shall only select an advertised combination.

b. A module may use the same host interface ID or the same media interface ID in multiple Applications.
c. For cases where a module supports a host electrical interface ID that is included in SFF-8024 but uses a media interface that is proprietary or not yet listed in the media interface advertising ID tables in SFF-8024, the module can use a null ID (00h=undefined) or a custom ID for the media that the module supplier has established, combined with the host electrical interface ID. The host electrical interface ID and lanes provide the required information for the host to interoperate with modules that have unfamiliar or vendor-specific media types and future technologies.

Examples of Application advertising scenarios are shown in Appendix B.

6.2.2 Logical Module Use – Data Paths

The module advertises a list of supported Applications in the Application Advertising Tables described in section 6.2.1.1. The host selects one or more Applications from the advertised options to configure the module for use. When an Application has been selected, the group of module resources that are associated with that Application instance are collectively referred to as a Data Path. All module resources associated with a Data Path are initialized and deinitialized as a group. Separate Data Paths are initialized and deinitialized independently.

For example, a module advertises an Application that consists of a CAUI-4 host electrical interface and a 100GBASE-SR4 media interface combination. In this example, the module could advertise support for one or two instances of the Application. Each instance of the Application selected by the host would be a separate Data Path, where each Data Path includes four host electrical lanes and four module media lanes and is independent of the other Data Path.

In a different example, a module advertises an Application that consists of a 400GAUI-8 host electrical interface and a 400GBASE-DR4 media interface combination, and a second Application that consists of a 100GAUI-2 host electrical interface and a 100GBASE-DR media interface combination. The host may select one instance of the first Application or up to four instances of the second Application. Each instance of each selected Application becomes a separate, independent Data Path.

6.2.3 Data Path Configuration – Control Sets

A Control Set is a group of registers that are used to provide configuration settings for use by the module during Data Path initialization. Configuration settings are available for each host lane.

The key configuration settings are the Application Select control registers, defined in Table 8-48 or Table 8-52. These registers allow the host to define one or more Data Paths by mapping desired Applications onto physical lanes in the module. The Application Select control registers include an ApSel code, a Data Path ID and an Explicit Control bit.

Each supported Application advertised in Table 8-13 and Table 8-39 is identified by an ApSel code. The host uses the ApSel code to assign that Application to one or more specific host lanes using the Application Select Control registers. Where an Application requires multiple lanes, the host shall write the same ApSel code into each lane of that Application. The host lanes used to define a Data Path are a physical reference point for that Data Path but not intended to limit the scope of resources associated with the Data Path. The module resources associated with the Data Path may be located anywhere in the module and may be shared with other host lanes or associated with a media interface in the memory map. An ApSel code of 0000b in an Application Select register indicates that the applicable host lane and its associated resources are not allocated to any data path. When the ApSel code in an Application Select register is 0000b, the Data Path ID and Explicit Control fields in that register may be ignored by the module.

The Data Path ID field in the Application Select control registers is used to specify the lowest numbered host lane in that Data Path. The host shall assign lane combinations that are in accordance with the Lane Assignment Options field advertised by the module for that Application. For a multi-lane data path the host shall write the same Data Path ID in all lanes of that Data Path.

The Explicit Control bit allows the host to indicate that the module should use the host-provided signal integrity values for the resources associated with that lane, instead of using Application-defined signal integrity values. When the Explicit Control bit is programmed as shown in Table 6-2, the associated signal integrity control field value for that lane is used during Data Path initialization. The signal integrity control field value for that lane is ignored for all other values of the Explicit Control bit, and the module shall instead use signal integrity settings that are compliant with the standard associated with the selected Application.

Table 6-2 Control field dependency on Explicit Control bit

Control field	Explicit Control value
Tx Adaptive Input Eq Enable	1
Tx Adaptive Input Eq Recall	1 or 0
Tx Input Eq control	1
Tx CDR control	1
Rx CDR control	1
Rx Output Eq control, pre-cursor	1
Rx Output Eq control, post-cursor	1
Rx Output Amplitude control	1

The usage of these signal integrity control fields is defined in section 6.2.4.

6.2.3.1 Control Set Usage

There are two types of control sets. The Active Control Set reports the current settings that are used by the module to control its hardware. The Staged Control Sets are used by the host to identify new settings for future use. Apply-fields are used to copy settings from Staged Control Set registers into Active Control Set registers. This apply mechanism decouples the timing and sequence of host writes to the Staged Control Set from the module actions used to configure the module hardware. Each module shall implement the Active Control Set and at least one host-configurable Staged Control Set.

When the host requests initialization of one or more data paths, the module uses the settings in the Active Control Set to initialize the resources associated with the appropriate data path. Those settings may have been copied from the Staged Control Set by a previous host Apply action, or those settings may have been programmed into the Active Set as power-on defaults. The module shall populate both Staged Control Set 0 and the Active Control Set registers with the module-defined default Application and signal integrity settings before exiting the MgmtInit state (see section 6.3.1.6). Module implementers should note that when the Application Select register is programmed to 0000b, that lane has no data path. The module should continue to report a Data Path Status of DataPathDeactivated for such lanes.

There are two controls that can be used to copy the settings from a Staged Control Set to the Active Control Set on a per lane basis: Apply_DataPathInit and Apply_Immediate. When used in the DataPathDeactivated State the Apply_DataPathInit and Apply_Immediate controls only copy the settings into the Active Control Set and do not cause a transition in the Data Path State Machine (see section 6.3.2 for Data Path State Machine details). When the host causes the DataPathDeinitS transition signal to become FALSE (see Table 6-15), the Data Path State Machine shall transition to DataPathInit, regardless of which Apply mechanism had been used.

When used in the DataPathInitialized or DataPathActivated State, the Apply_DataPathInit control copies the Staged Control Set into the Active Control Set and performs a full re-initialization of the data path. In this scenario, the Apply action must be performed on all lanes in the data path at the same time. Use of Apply_DataPathInit in the DataPathActivated state may be disruptive because the Data Path State Machine returns to DataPathInit, where the transmitters are disabled. In cases where new settings need to be applied quickly without disabling the transmitters, such as Fibre Channel Link Speed Negotiation (LSN), the host should use the Apply_Immediate control. This control does not transition the Data Path State Machine out of

DataPathInitialized or DataPathActivated. Host implementers should note that the host is required to transition the data path state to DataPathDeactivated before the host selects an Application with a different lane count.

The module may report the acceptance or rejection of the requested configuration using the Configuration Error Code registers in Table 8-63. If accepted, the module copies the configuration into the Active Set and changes the data path state. If the configuration is rejected, the module aborts the Apply operation without copying the settings. The Configuration Error Code is reported on all applicable lanes and may differ from data path to data path.

Figure 6-2 illustrates the flow of Control Set settings from the Staged Set into the Active set and module hardware.

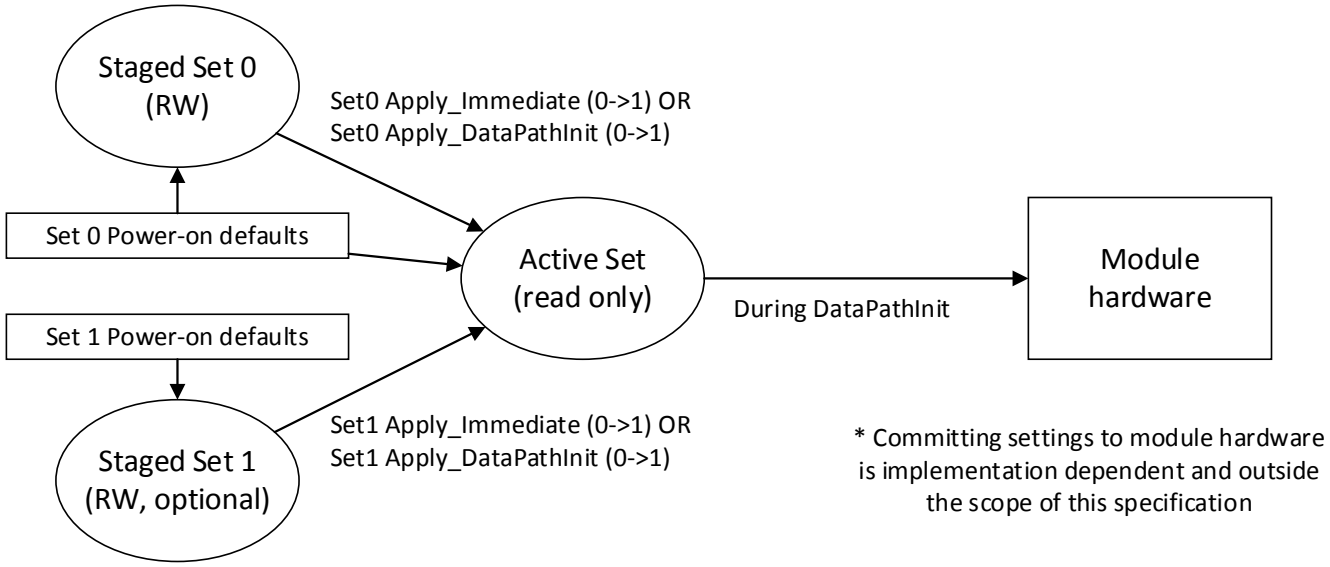


Figure 6-2 Control Set Data Flow Diagram

The translation of memory map settings to the module hardware is implementation-specific and outside the scope of this specification. Module implementers should use a best effort approach when trying to translate memory map settings to module hardware settings.

If the host sets the same bits in both Apply_DataPathInit and Apply_Immediate in the same two-wire serial transaction, the Apply_DataPathInit bit shall take precedence. The host shall not set bits for Apply_DataPathInit or Apply_Immediate when the corresponding data path is in DataPathInit, DataPathDeinit, DataPathTxTurnOn, or DataPathTxTurnOff; the module may ignore such requests.

Host implementers shall adhere to the following rules when using Control Sets:

- The host shall not change the data path width without first transitioning the data path to the DataPathDeactivated state.
- The host shall not Apply staged control set lanes where the Application Select register is set to an ApSel of 0000b unless the associated data path is in the DataPathDeactivated state.
- A valid ApSel shall be assigned to all host lanes in the Active Set at all times
- ApSel = 0000b shall be assigned to each individual unused host lane.

6.2.3.2 Initialization Sequence Examples

The data path architecture described above is intentionally designed to support a broad array of implementations while ensuring compatibility across hosts and modules. Some Applications may not use all of the features provided in the architecture.

Appendix A contains some example host-module initialization flows that can be used for popular Applications.

6.2.4 Signal Integrity Controls

Memory map signal integrity control fields provide a mechanism for the host to override the default signal integrity settings defined by an Application. These signal integrity overrides are only copied to the Active Set (and subsequently committed to module hardware, see Figure 6-2) if the Explicit Control bit is 1 in the applicable Staged Control Set (see Table 8-48 and Table 8-52) when either Apply_DataPathInit on Apply_Immediate is used. If the Explicit Control bit is 0, the module writes the Application-defined default signal integrity values into the Active Set on an Apply operation. For all signal integrity controls, the host sets the code for the desired behavior and the device makes a best effort to provide the function indicated.

6.2.4.1 Tx Input Equalization Control

The Tx Input Equalizer has multiple controls associated with it. These controls can be divided into two groups: those that are active when Tx Adaptive Input Eq is enabled and those that are active when Tx Adaptive Input Eq is disabled. Table 6-3 summarizes which controls are associated with each group. The module shall ignore the value in the applicable control field when the Tx Adaptive Input Eq Enable bit is not set to use that control.

Table 6-3 Tx Input Eq control relationship to Tx Adaptive Input Eq Enable

Control	Tx Adaptive Input Eq Enable value to use this control
Tx Input Eq Adaptation Freeze	1
Tx Input Eq Adaptation Store	1
Tx Adaptive Input Eq Recall	1
Tx Input Eq control	0

The Tx Input Equalization Control is a four-bit field per lane as shown in Table 6-4. This field allows the host to specify fixed Tx input equalization and is ignored by the module if Tx Adaptive Input Eq Enable is set for that lane. Refer to Table 8-34 to determine if the module supports Fixed Tx Input Equalization Control. Refer to Table 8-30 for the Maximum Tx equalization supported by the module. The code values and the corresponding input equalization are based on a reference CTLE and may not directly apply to the equalizer implemented in the module.

Table 6-4 Fixed Tx Input Equalization Codes

Code Value	Bit pattern	Input Equalization
0	0000b	No Equalization
1	0001b	1 dB
2	0010b	2 dB
3	0011b	3 dB
4	0100b	4 dB
5	0101b	5 dB
6	0110b	6 dB
7	0111b	7 dB
8	1000b	8 dB
9	1001b	9 dB
10	1010b	10 dB
11	1011b	11 dB
12	1100b	12 dB
13-15		Custom

6.2.4.2 Rx Output Emphasis Control

The Rx Output Emphasis Control is a four-bit field per lane. Refer to Table 8-34 to determine if the module supports Rx Output Emphasis Control. Refer to Table 8-30 for the maximum Rx output emphasis supported by the module. Rx output emphasis is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output equalization are defined as follows:

Table 6-5 Rx Output Emphasis Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000b	No Equalization	No Equalization
1	0001b	1 dB	0.5 dB
2	0010b	2 dB	1.0 dB
3	0011b	3 dB	1.5 dB
4	0100b	4 dB	2.0 dB
5	0101b	5 dB	2.5 dB
6	0110b	6 dB	3.0 dB
7	0111b	7 dB	3.5 dB
8-10	1000b-1010b	Reserved	Reserved
11-15	1011b-1111b	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB)=-20*log10((1-C(-1)/(C(-1)+C(0)+C(1)))
The post-cursor equalizer settings in dB approximates to
Post EQ (dB)=-20*log10(1-C(1)/(C(-1)+C(0)+C(1)))

6.2.4.3 Rx Output Amplitude Control

The Rx Output Amplitude Control is a four-bit field per lane. The output amplitude is measured with no equalization enabled. Refer to Table 8-34 to determine if the module supports Rx Output Amplitude Control and Table 8-30 to determine which codes are supported. Output amplitude is defined at the appropriate test point defined by the relevant standard. The code values and the corresponding output amplitude are defined as follows:

Table 6-6 Rx Output Amplitude Codes

Code Value	Bit pattern	Output Amplitude
0	0000b	100-400 mV (P-P)
1	0001b	300-600 mV (P-P)
2	0010b	400-800 mV (P-P)
3	0011b	600-1200 mV (P-P)
4-14	0100b-1110b	Reserved
15	1111b	Custom

6.2.4.4 Tx Input Eq Adaptation Store/Recall Methodology

Transmit equalizer adaptation can be a time-consuming activity. In some implementations, the available time for a speed change does not include equalizer adaptation time. This specification provides an optional Tx Input Eq Adaptation Store and Recall mechanism, to facilitate storing of adapted equalizer values for recall and use at a later time.

Module support of the Tx input Eq Adaptation Store and Recall mechanism is optional and declared in Table 8-34. This advertisement field identifies the number of Store/Recall buffers implemented in the module. These buffers are independent of Staged Set 0 and 1 and may be numbered independently. The module shall provide sufficient storage in each Store/Recall buffer to store the adapted equalizer value for each lane in the module. This storage is implementation specific and not defined in this specification.

The Tx Input Eq Adaptation Store control field is located in Table 8-46. This field provides two bits per lane and is write only. A read of this register shall return 0. When the host would like to store the most recent adapted Tx input equalizer value, the host shall write the target store location encoding into the Tx Input Eq Adaptation Control, into each lane whose adapted value should be stored. Adaptation shall continue to occur after the store event completes unless the Tx Input Eq Adaptation Freeze bit is set. Host requests to store the Tx Input Eq Adaptation when the Tx Input Eq Adaptation Enable bit for that lane is clear shall be ignored by the module. Tx Input Eq Adaptation Store may occur at any time while the data path state is in DataPathInitialized or DataPathActivated and occurs when requested.

The Tx Input Eq Adaptation Recall control field is located in Table 8-49 for Staged Set 0 and Table 8-53 for Staged Set 1. This field provides two bits per lane and is read-write. The Active Set provides a read-only indication of the current Tx Input Eq Adaptation Recall status for each lane. The host may recall any stored Tx Input Eq Adaptation by programming the applicable lane controls with the store location to be recalled. These values are not recalled until the Apply_DataPathInit or Apply_Immediate bits are 1 for that Staged Set.

The Tx Input Eq Adaptation Recall field is used independent of the Explicit Control field settings for that lane. If the Tx input freeze bit is clear, the recalled Tx input Eq adaptation shall be used as the starting point for continuous adaptation for the applicable lanes. If the Tx Input Eq Freeze bit is set, the recalled Tx Input Eq Adaptation shall be used as the frozen Tx Input Eq value for the applicable lanes.

6.3 Module Behavioral Model

Critical power up and initialization interactions between the host and module are described using state machine behavioral models. These state machines are intended to specify required software behaviors, not software implementation techniques.

Two state machine types are used in this document. A single module-level state machine defines module-wide characteristics, such as the initialization of the management interface and the module power mode. A data path state machine defines the host and module interactions and behaviors needed for initialization of a data path which can be an individual lane or group of lanes in the module. As there can be multiple data paths in the module, there can be multiple data path state machines. For more on data paths see section 6.3.2.

In both module and data path state machines, there are two kinds of states. States where the module is waiting for module hardware or the host to initiate action are referred to as 'steady states'. States that progress to completion without host action are referred to as 'transient states'. In the state machine illustrations, Figure 6-3, Figure 6-4 and Figure 6-5, the steady states have a rectangular outline and the transient states have an oval outline. The durations of steady states are unbounded while the maximum durations of transient states are implementation-dependent and, in some cases, advertised by the module. Dynamic register content may be unreliable during transient states.

This common management interface specification is designed to be applied to multiple form factors. Therefore, actions and properties are described using generic terms instead of using application-specific signal names. Refer to Appendix A for the association between generic descriptors in this section and application-specific signal names.

6.3.1 Module State Machine

The Module State Machine is used by the module to communicate the availability of module-wide interfaces to the host. Through the Module State Machine, the host can determine when the management interface has completed initialization after power on or on exit from reset. The host can also use the Module State Machine to determine when the high-speed circuitry in paged memory modules is fully powered such that the host can initialize data paths through the Data Path State Machine, described in section 6.3.2.

The Module State Machine is engaged after module insertion and power on. The Module State Machine is applicable to both modules and cable assemblies, whether passive or active. The Module State Machine for devices implementing a paged memory map is described in section 6.3.1. The Module State Machine for devices implementing a flat (non-paged) memory map is described in section 6.3.1.2. Modules that implement a read-only memory map typically utilize the flat memory model. Modules that implement read-write memory maps should use the paged memory map model.

The Module State Machine describes module-wide behaviors and properties. For data path-specific behaviors and properties, refer to the Data Path State Machine in section 6.3.2.

6.3.1.1 Module State Machine, paged memory modules

Modules that implement a paged memory map shall adhere to the behaviors described by the Module State Machine shown in Figure 6-3.

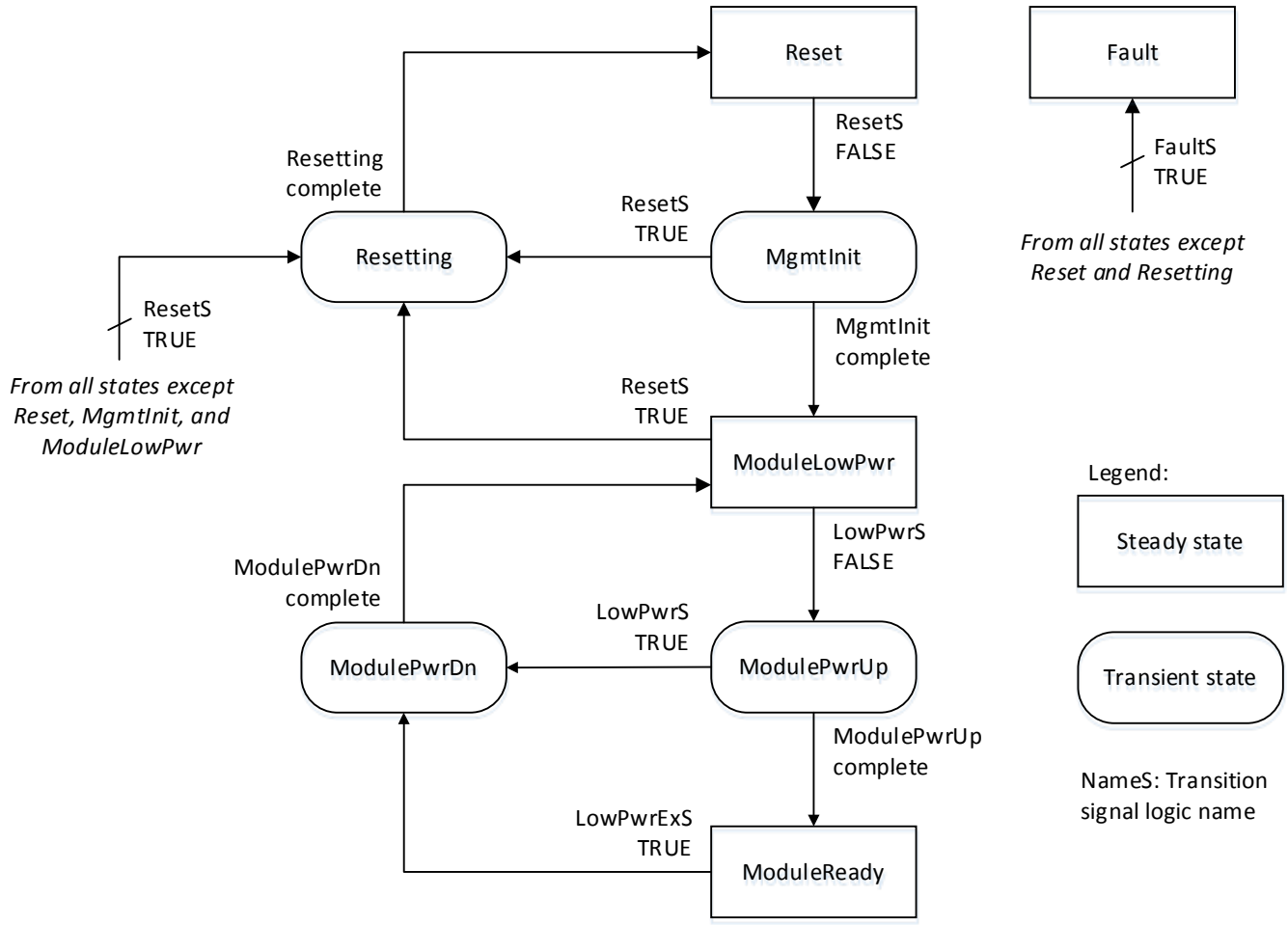


Figure 6-3 Module State Machine, paged memory modules

On module power-up, the Module State Machine is in the Reset state if ResetS is TRUE. Otherwise, the Module State Machine transitions to the MgmtInit state.

The state machine exits a given state when specific conditions are satisfied. Transition signals (names ending in S) are used to summarize a logic condition. The following table describes the priority of exit conditions, if more than one exit condition is satisfied at the same time. Note that not all exit conditions are applicable to all states.

Table 6-7 Module State Machine exit condition priority

Priority	Exit Condition
1	ResetS
2	FaultS
3	All other exit conditions

The ResetS transition signal is described using the truth table shown in Table 6-8, below.

Table 6-8 ResetS transition signal truth table

VccResetL (due to low Vcc)	ResetL hardware signal	Software Reset see Table 8-7	ResetS transition signal
0	X	X	1
1	0	X	1
1	1	1	1
1	1	0	0

The ResetS transition signal can also be represented by the logic equation

ResetS = NOT VccResetL OR NOT ResetL OR Software Reset

VccResetL is defined as the circumstance where the voltage of one or more of the Vcc power rails as observed at the module input drops below an implementation-defined minimum value. Implementation of VccResetL is optional. ResetL, as described in is an active-low signal, and must be asserted for longer than the minimum reset pulse duration to trigger a module reset. Refer to form factor-specific documentation for the minimum reset pulse duration.

The FaultS transition signal truth table and logic equation are module implementation-specific.

The LowPwrS transition signal is described using the truth table shown in Table 6-9, below.

Table 6-9 LowPwrS transition signal truth table

ForceLowPwr see Table 8-7	LowPwr see Table 8-7	LPMode hardware signal	LowPwrS transition signal
1	X	X	1
0	1	1	1
0	1	0	0
0	0	1	0
0	0	0	0

The LowPwrS transition signal can also be represented by the logic equation

LowPwrS = ForceLowPwr OR (LowPwr AND LPMode)

The LowPwrExS transition signal is described using the truth table shown in Table 6-10, below. This transition signal is used to control exit from the ModuleReady state, which occurs when both the LowPwrS transition signal is TRUE and all data paths have reached the DataPathDeactivated state.

Table 6-10 LowPwrExS transition signal truth table

LowPwrS transition signal	Module DeactivatedT	LowPwrExS transition signal
1	1	1
1	0	0
0	1	0
0	0	0

The LowPwrExS transition signal can also be represented by the logic equation

LowPwrExS = LowPwrS AND ModuleDeactivatedT

where

ModuleDeactivatedT = (Lane 1 Data Path State = DataPathDeactivated) AND
(Lane 2 Data Path State = DataPathDeactivated) AND ...
(Lane N Data Path State = DataPathDeactivated)
N = number of host lanes in the module

Table 6-11 provides a summary of the high-level behaviors and properties of each module state for paged memory module implementations. Refer to sections 6.3.1.4-6.3.1.11 for detailed requirements for each state.

Table 6-11 Module state behaviors, paged memory modules

State	Power Mode	Behavior in state	Exit condition	Next state	Required/ Optional
Resetting	High/ Low Power	Management interface and all module electronics transition to reset	Resetting completed	Reset	Required
Reset	Low Power	Management interface and all module electronics in reset	ResetS transition signal becomes FALSE	MgmtInit	Required
MgmtInit	Low Power	Management interface powering up and initializing	ResetS transition signal becomes TRUE	Resetting	Required
			FaultS transition signal becomes TRUE	Fault	
			Module management interface ready OR t_init timeout (See Hardware Specification)	ModuleLowPwr	
ModuleLowPwr	Low Power	Management interface available, host may configure module	ResetS transition signal becomes TRUE	Resetting	Required
			FaultS transition signal becomes TRUE	Fault	
			LowPwrS transition signal becomes FALSE	ModulePwrUp	
ModulePwrUp	High Power	Module transitioning to high power mode	ResetS transition signal becomes TRUE	Resetting	Required
			FaultS transition signal becomes TRUE	Fault	
			LowPwrS transition signal becomes TRUE	ModulePwrDn	
			Power up activities are complete	ModuleReady	
ModuleReady	High Power	Module may be consuming power up to the level defined in the fields in Table 8-18	ResetS transition signal becomes TRUE	Resetting	Required
			FaultS transition signal becomes TRUE	Fault	
			LowPwrExS transition signal becomes TRUE	ModulePwrDn	
ModulePwrDn	High Power	Module transitioning to low power mode	ResetS transition signal becomes TRUE	Resetting	Required
			FaultS transition signal becomes TRUE	Fault	
			Module has returned to Low Power mode	ModuleLowPwr	
Fault	*Low Power	Module is waiting for host action	Module power down	N/A	Optional
			ResetS transition signal becomes TRUE	Resetting	

*It is suggested, if possible, that the Fault state be in Low Power mode.

Certain Module State Machine state transitions cause the Module State Changed flag to be set, while other transitions do not set this flag. In general, module-initiated state transitions result in the Module State Changed flag being set. Table 6-12 below defines the appropriate flag behavior for each valid state transition. If the exit criteria for the new state is met upon entry into the state, the Module State Change flag shall not be set. In such

cases, the flag will be set when the Module State completes the multi-step transition sequence, to avoid generation of intermediate state change interrupts to the host.

Table 6-12 Module State Changed flag behaviors

Prior state	Next state	Causes Module State Changed flag to be set?
Fault	Resetting	No
Resetting	Reset	No
Reset	MgmtInit	No
Any state	Resetting	No
Any state	Fault	Yes
MgmtInit	ModuleLowPwr	Yes*
ModuleLowPwr	ModulePwrUp	No
ModulePwrUp	ModuleReady	Yes
ModulePwrUp	ModulePwrDn	No
ModuleReady	ModulePwrDn	No
ModulePwrDn	ModuleLowPwr	Yes

*if the exit condition is not met on entry into the state

6.3.1.2 Module State Machine, flat memory modules

Modules that implement a flat memory map shall adhere to the behaviors described by the Module State Machine shown in Figure 6-4. All other modules shall implement the behaviors described by the Module State Machine for paged memory modules, defined in section 6.3.1.1.

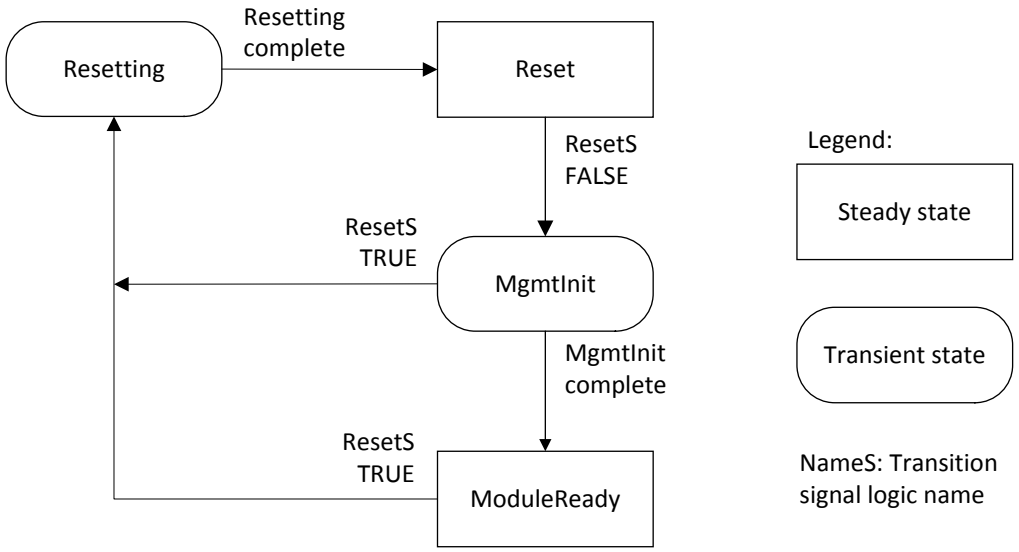


Figure 6-4 Module State Machine, flat memory modules

As shown in Figure 6-4, flat memory modules transition to the ModuleReady state without host interaction. Module state transitions for flat memory modules are a specification formalism, since the contents of the static EEPROM-based memory map does not change. Although the behaviors of the Resetting, Reset, and MgmtInit states apply to such modules, those states are not reported to the host through the memory map. Flat memory modules shall statically advertise a module state of ModuleReady (see Table 8-2).

The ResetS transition signal is described in Table 6-8. For flat memory modules, assertion of the ResetL signal may optionally hold the EEPROM in reset, however the data path shall remain active. Flat memory modules are not required to support Software Reset or VccResetL.

At initial module insertion or application of power, the Module State Machine initializes to the Reset state. Table 6-13 provides a summary of the high-level behaviors and properties of each module state for flat memory modules. Refer to sections 6.3.1.4-6.3.1.11 for detailed requirements for each state.

Table 6-13 Module state behaviors, flat memory modules

State	Power Mode	Behavior in state	Exit condition	Next state	Required/ Optional
Resetting	Low Power	Management interface transitions to reset	Resetting completed	Reset	Optional
Reset	Low Power	Management interface in reset	ResetS transition signal becomes TRUE	MgmtInit	Optional
MgmtInit	Low Power	Management interface powering up and initializing	ResetS transition signal becomes TRUE	Resetting	Required
			Module Management Interface ready AND Interrupt signal asserted OR t_init timeout. (See Hardware Specification)	ModuleReady	
ModuleReady	Low Power	Management interface available	ResetS transition signal becomes TRUE	Resetting	Required

6.3.1.3 Module Power Mode control

The Module Power Mode dictates the maximum power that the module is permitted to consume. The Module Power Mode is a function of the state of the Module State Machine. Two Module Power Modes are defined: Low Power Mode and High Power Mode. The maximum module power consumption in Low Power Mode is defined in the form factor-specific hardware specification. The maximum module power consumption in High Power Mode is module implementation dependent and is advertised in Table 8-18.

All modules initially boot in Low Power Mode, while the module is transitioning through the MgmtInit state. After the management interface has been initialized, the host may transition paged memory modules to High Power Mode using the conditions defined by the LowPwrS transition signal (see Table 6-9). If LowPwrS is FALSE when the module is in the ModuleLowPwr state, the module shall begin power up procedures defined by the ModulePwrUp state (section 6.3.1.8). Conversely, when LowPwrS (or LowPwrExS, as applicable) becomes TRUE, the module begins the transition back to the ModuleLowPwr state and Low Power Mode, using the power down procedures defined by the ModulePwrDn state (section 6.3.1.10).

The LowPwrS transition signal only controls the power mode of the module and not data path initialization. Refer to section 6.3.2 for Data Path State Machine details.

6.3.1.4 Resetting State

The Resetting state is a transient state used by the module to gracefully power down module electronics before entering the Reset state. The Resetting state initiates a complete module reset. The shutdown procedure used by the module for a reset event is implementation dependent. The module may be in High Power Mode during portions of the Resetting state.

The Resetting state is entered from any state except the Reset state when the ResetS transition signal is TRUE. The ResetS transition signal is defined in Table 6-8.

When a paged memory module enters the Resetting state, all Data Path State Machines are torn down. Refer to section 6.3.2 for Data Path State Machine behaviors.

Management interface transactions initiated by the host during the Resetting state may be ignored by the module. Transactions in progress may be aborted when entering the Resetting state. Note: While the ResetS transition signal is TRUE, the management interface may be held in reset and may not respond (NACK).

When all module electronics have been powered down and are in reset, the module state transitions to the Reset state.

6.3.1.5 Reset State

The Reset state is a steady state. The module shall remain in the Reset state as long as the ResetS transition signal is TRUE (see Table 6-8). All internal module electronics shall be placed in reset upon entry into the Reset state for the duration of the state. On entry into the Reset state, the Software Reset bit (Table 8-7) returns to its default value. Note this means that the module hardware implementation must have some mechanism to clear this bit when in the Reset State or upon exiting the Reset State. All other bits are set to their power-up default values in the MgmtInit State, regardless of their value when exiting the Reset State.

The module shall remain in Low Power mode throughout the Reset state. All interrupts shall be suppressed while the module is in the Reset state.

Management interface transactions initiated by the host during the Reset state may be ignored by the module. Transactions in progress may be aborted when entering the Reset state. Note: While the ResetS transition signal is TRUE, the management interface may be held in reset and may not respond (NACK).

After the ResetS transition signal becomes FALSE, the module may not respond until the MgmtInit state is complete. The Reset state can only be exited if the ResetS transition signal is FALSE and power is applied. Upon exit from the Reset state, the module enters the MgmtInit state.

6.3.1.6 MgmtInit State

The MgmtInit state is a transient state that is entered any time the module is brought out of the Reset state, (either hardware or software reset). The MgmtInit state is applicable to both paged memory modules and flat memory modules.

During this state, the module configures the memory map and initializes the management interface for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power Mode throughout this state. For paged memory modules, all Data Path States shall remain in DataPathDeactivated throughout MgmtInit. The module may ignore all TWI transactions while in the MgmtInit state.

Interrupt flag conformance in the MgmtInit state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during MgmtInit.

Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. The module shall have completed MgmtInit within the module form-factor dependent management interface initialization time, defined as the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in the form factor-dependent specification), hot plug, or the rising edge of the Reset signal until the module has configured the memory map to default conditions and activated the management interface.

Upon completion of MgmtInit, the next state is ModuleLowPwr.

6.3.1.7 ModuleLowPwr State

The ModuleLowPwr state is a steady state, where the management interface is fully initialized and operational and the device is in Low Power Mode. During this state, the host may configure the module using the management interface and memory map. Some examples of configuration activities include reading the ID and device property fields, setting CDR and other lane attributes and configuration of monitor masks. Details of host-module interactions in the ModuleLowPwr state are implementation dependent and are outside the scope of this specification.

Upon entry into the ModuleLowPwr state, the module shall set the Module State register (Table 8-2) to the ModuleLowPwr state and set the Module State Changed interrupt flag (Table 8-5) only if the ModuleLowPwr exit criteria are not met upon entry into the state. The module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag.

Interrupt flag conformance in the ModuleLowPwr state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during ModuleLowPwr.

The Data Path State for all lanes shall remain in DataPathDeactivated throughout the ModuleLowPwr state.

The module state transitions to ModulePwrUp when the LowPwrS transition signal is FALSE (see Table 6-9). This transition can occur at any time during ModuleLowPwr, and so modules shall regularly sample LowPwrS throughout the ModuleLowPwr state[1]. In some implementations, the LowPwrS transition signal may evaluate to 0 the first time it is sampled in ModuleLowPwr. Host implementers should note that, in such circumstances, the transition to ModulePwrUp may be too fast for the host to detect that the module was in the ModuleLowPwr state.

6.3.1.8 ModulePwrUp state

The ModulePwrUp state is a transient state used to inform the host that the module is in the process of powering up to High Power Mode.

Entry into ModulePwrUp occurs from ModuleLowPwr, when the LowPwrS transition signal is FALSE (see Table 6-9). Upon entry into ModulePwrUp, the module shall set the Module State register (Table 8-2) to the ModulePwrUp state.

The module may be in High Power mode at any time during the ModulePwrUp state.

Interrupt flag conformance in the ModulePwrUp state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during ModulePwrUp. However, the module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag.

The Data Path State for all lanes shall remain in DataPathDeactivated throughout the ModulePwrUp state.

If the LowPwrS transition signal is TRUE at any time during the ModulePwrUp state, the module state immediately transitions to ModulePwrDn.

When the module power up sequence has completed, the module state transitions to the ModuleReady state.

6.3.1.9 ModuleReady State

The ModuleReady state is a steady state that indicates that the module is in High Power mode. When the module state is ModuleReady, the host may initialize or deinitialize data paths.

[1] Note: this behavior differs from the behaviors defined in CMIS 3.0

Upon entry into the ModuleReady state, the module shall set the Module State register (Table 8-2) to the ModuleReady state and set the Module State Changed interrupt flag (Table 8-5). The module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag.

Interrupt flag conformance in the ModuleReady state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during ModuleReady.

The only non-Reset or Fault action that results in an exit from ModuleReady is if the LowPwrExS transition signal is TRUE (see Table 6-10), which causes the module state to transition to ModulePwrDn.

6.3.1.10 ModulePwrDn State

The ModulePwrDn state is a transient state that is used to inform the host that the module is in the process of returning to Low Power mode.

Upon entry into the ModulePwrDn state, the module shall set the Module State register (Table 8-2) to the ModulePwrDn state.

The module may be in High Power mode at any time during the ModulePwrDn state.

Interrupt flag conformance in the ModulePwrDn state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during ModulePwrDn. However, the module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag.

The Data Path State for all lanes shall remain in DataPathDeactivated throughout the ModulePwrDn state.

When the module is in Low Power Mode, the module shall transition to the ModuleLowPwr state. Implementers should note that modules in ModulePwrDn shall ignore the LowPwrS transition signal, so if this signal is FALSE during ModulePwrDn, the module will complete the power-down sequence and transition to ModuleLowPwr before sampling LowPwrS again.

6.3.1.11 Fault State

The Fault state is provided for notification to the host that a module fault has occurred. Definition of the Fault state is implementation dependent. The Fault state shall only be entered when module detects a condition (e.g. TEC runaway, memory corruption) that could cause damage. The specification intent of the Fault state is to put the module in a condition that does not create further equipment failures. It is recommended that the module enter Low Power mode during the Fault state but the response to a Fault condition is implementation specific.

The only exit path from the Fault state is to perform a module reset by taking an action that causes the ResetS transition signal to become TRUE (see Table 6-8).

6.3.2 Data Path State Machine

A data path is defined as a combination of one or more host lanes, one or more media lanes, and a set of internal module resources that are collectively identified by a single selected Application. Data paths are only applicable to paged memory modules.

The Data Path State Machine(s) are set-up (come into existence) during MgmtInit, based on the power-up default Application Select field values in the Active Set. The Data Path State Machine(s) are in the DataPathDeactivated State until the Module State Machine is in the ModuleReady state, and the exit condition from the DataPathDeactivated state is met. Updating the Application Select fields in the Active Set, in either the ModuleLowPwr or ModuleReady states, tears down previous Data Path State Machine(s) that are no longer defined and sets up the newly-defined Data Path State machine(s). All Data Path State Machines are also torn down in the Resetting state.

Refer to section 6.3.1 for an overview of the Module State Machine, section 6.2.1 for an overview of Applications, section 6.2.2 for an overview of Data Paths, and section 6.2.3 for an overview of Control Sets.

The Data Path State Machine is used by the module to communicate the initialization status of the resources associated with a data path. Although individual resources within a data path may complete initialization activities at different times, the module shall wait to report the updated data path state until all resources associated with the data path have completed the requested action. This synchronized status reporting across all lanes and resources in a data path means that there is one Data Path State Machine per data path. This specification describes the behavioral model to be used for each Data Path State Machine. A variety of module implementations that meet this behavioral model are possible but are outside the scope of this specification.
Some example data path initialization flows that comply with the Data Path State Machine behavioral model are provided in Appendix B. Modules identify supported data path configuration options through the Application advertisement fields.

Each data path is required to operate independently of other data paths: if the host changes the Data Path State of one data path, the other data paths in the module shall be unaffected and uninterrupted. Module implementers should note that independent operation of data paths may require independent clocking per data path, from a recovered clock within that data path. See the applicable hardware specification for further information. The module shall only advertise Applications and lane configurations that are supported by the implemented clocking scheme. Figure 6-5 shows the Data Path State Machine for one data path instance.

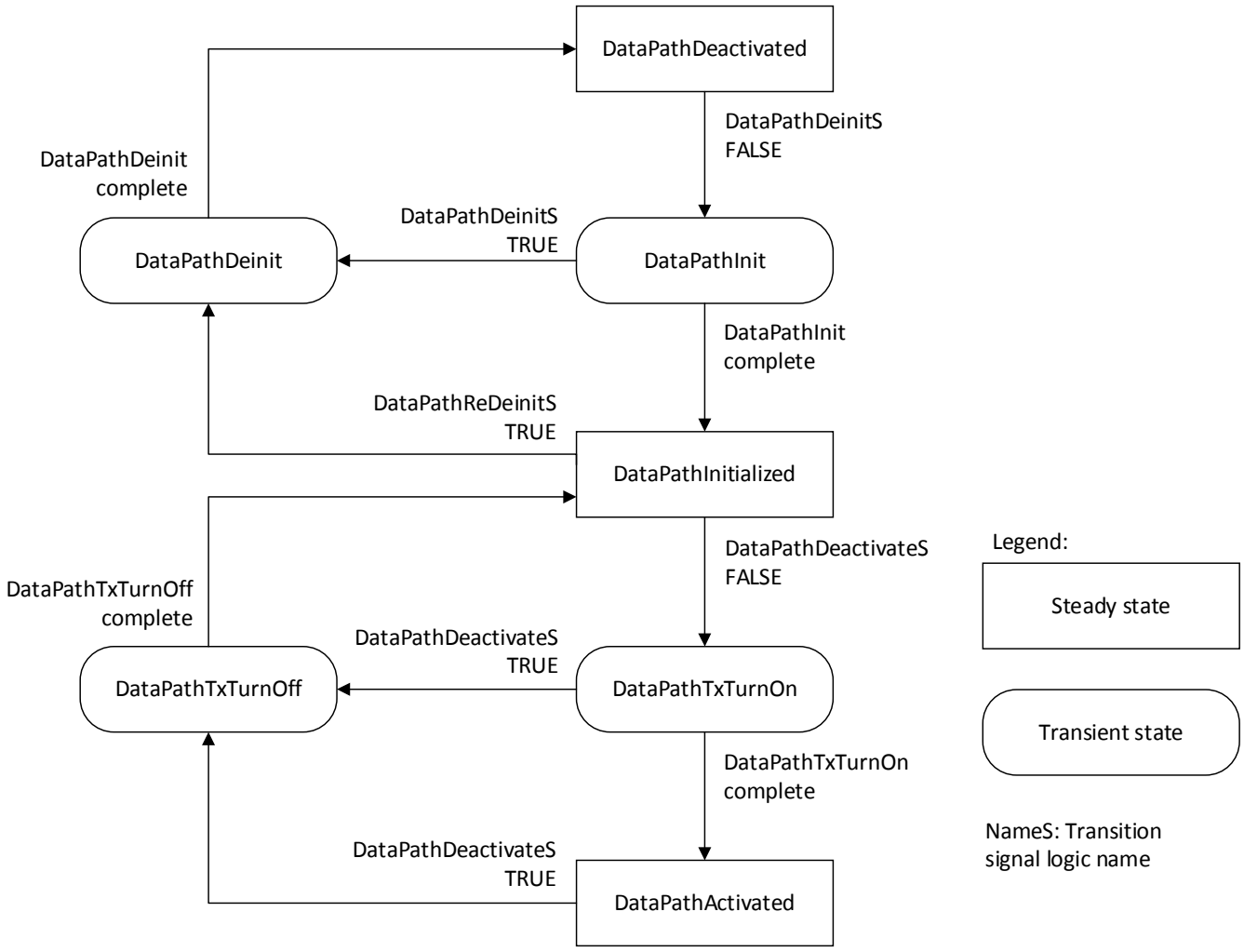


Figure 6-5 Data Path State Machine

The Data Path State Machine describes data path-specific behaviors and properties. For module-wide behaviors and properties, refer to the Module State Machine in section 6.3.1.

Prior to exit from the MgmtInit module state, all data paths initialize to the DataPathDeactivated state.

The state machine exits a given state when specific conditions are satisfied. Transition signals (names ending in S) are used to summarize a logic condition. The following table describes the priority of exit conditions, if more than one exit condition is satisfied at the same time. Note that not all exit conditions are applicable to all states.

Table 6-14 Data Path State Machine exit condition priority

Priority	Exit Condition
1	ResetS
2	FaultS
3	All other exit criteria

The DataPathDeinitS transition signal is described using the truth table shown in Table 6-15, below.

Table 6-15 DataPathDeinitS transition signal truth table

ModuleReadyT	LowPwrS see Table 6-9	DataPathDeintT	DataPathDeinitS transition signal
0	X	X	1
1	1	X	1
1	0	1	1
1	0	0	0

The DataPathDeinitS transition signal can also be represented by the logic equation

DataPathDeinitS = NOT ModuleReadyT OR LowPwrS OR DataPathDeinitT

where

ModuleReadyT = (Module State = ModuleReady)
DataPathDeinitT = (DataPathDeinit Lane N) OR
(DataPathDeinit Lane N+1) OR ...
(DataPathDeinit Lane N+M-1)
N = first host lane in the data path
M = number of host lanes in the data path

The DataPathReDeinitS transition signal is described using the truth table shown in Table 6-16, below.

Table 6-16 DataPathReDeinitS transition signal truth table

DataPathDeinitS transition signal	DataPathReinitT	DataPathReDeinitS transition signal
1*	1*	1
1	0	1
0	1	1
0	0	0

*DataPathDeinitS and DataPathReinitT cannot be 1 at the same time

The DataPathReDeinitS transition signal can also be represented by the logic equation

DataPathReDeinitS = DataPathDeinitS OR DataPathReinitT

where

DataPathReinitT = (Lane N Apply_DataPathInit) OR
(Lane N+1 Apply_DataPathInit) OR ...
(Lane N+M-1 Apply_DataPathInit)
N = first host lane in the data path
M = number of host lanes in the data path

The DataPathDeactivateS transition signal can be represented by the logic equation

DataPathDeactivateS = DataPathReDeinitS OR DataPathTxDisableT OR DataPathTxForceSquelchT

where

DataPathTxDisableT = (TxN Disable) OR
(TxN+1 Disable) OR ...
(TxN+M-1 Disable)
DataPathTxForceSquelchT = (TxN Force Squelch) OR

(TxN+1 Force Squelch) OR ...
(TxN+M-1 Force Squelch)
N = first media lane in the data path
M = number of media lanes in the data path

Implementers should note that disabling or forcing squelch on one lane in a data path will cause the entire data path to transition to DataPathInitialized. Although some lanes may continue to be enabled while in DataPathInitialized, since not all lanes are enabled, the data path is considered not activated.

Table 6-17 provides a summary of the high-level behaviors and properties of each data path state. Refer to sections 6.3.2.2-6.3.2.8 for detailed requirements for each state.

Table 6-17 Data path state behaviors

State	Tx output state	Exit condition	Next State
DataPathDeactivated	Quiescent	DataPathDeinitS transition signal becomes FALSE	DataPathInit
DataPathInit	Quiescent	ResetS transition signal becomes TRUE	DataPathDeactivated
		DataPathDeinitS transition signal becomes TRUE	DataPathDeinit
		Module completes data path initialization	DataPathInitialized
DataPathInitialized	Depends on per-lane Tx Disable and Tx Force Squelch	ResetS transition signal becomes TRUE	DataPathDeactivated
		DataPathReDeinitS transition signal becomes TRUE	DataPathDeinit
		DataPathDeactivateS transition signal becomes FALSE	DataPathTxTurnOn
DataPathDeinit	Quiescent	ResetS transition signal becomes TRUE	DataPathDeactivated
		Data path deinitialization complete	DataPathDeactivated
DataPathTxTurnOn	In transition	ResetS transition signal becomes TRUE	DataPathDeactivated
		DataPathDeactivateS transition signal becomes TRUE	DataPathTxTurnOff
		Module Tx output is enabled and stable	DataPathActivated
DataPathActivated	Enabled	ResetS transition signal becomes TRUE	DataPathDeactivated
		DataPathDeactivateS transition signal becomes TRUE	DataPathTxTurnOff
DataPathTxTurnOff	In transition	ResetS transition signal becomes TRUE	DataPathDeactivated
		Module Tx output is squelched or disabled	DataPathInitialized

The Rx output state is not controlled by the Data Path State Machine. The host may control the Rx output using the Rx Output Disable control (Table 8-46).

As shown in Figure 6-5, if the ResetS transition signal (see Table 6-8) becomes TRUE during any state, the data path state transitions to DataPathDeactivated without transitioning through DataPathDeinit. In this scenario, any data path-specific power down activities should be performed as part of the Resetting module state.
Certain Data Path State Machine state transitions shall cause the Data Path State Changed flag to be set, while other transitions shall not set this flag. In general, module-initiated state transitions result in the Data Path State Changed flag being set. Table 6-18 below defines the appropriate flag behavior for each valid state transition.

Table 6-18 Data Path State Change flag behaviors

Prior state	Next state	Causes Data Path State Changed flag to be set?
DataPathDeactivated	DataPathInit	No
DataPathInit	DataPathInitialized	Yes*
DataPathInit	DataPathDeinit	No
DataPathInit	DataPathDeactivated	(on ResetS) No
DataPathInitialized	DataPathDeinit	No
DataPathInitialized	DataPathDeactivated	(on ResetS) No
DataPathDeinit	DataPathDeactivated	Yes*
DataPathTxTurnOn	DataPathActivated	Yes
DataPathTxTurnOn	DataPathTxTurnOff	No
DataPathTxTurnOn	DataPathDeactivated	(on ResetS) No
DataPathActivated	DataPathTxTurnOff	No
DataPathActivated	DataPathDeactivated	(on ResetS) No
DataPathTxTurnOff	DataPathInitialized	Yes*
DataPathTxTurnOff	DataPathDeactivated	(on ResetS) No

*if the exit condition is not met on entry into the state

There are circumstances when steady state exit conditions are already met upon entry into the state. An example of this scenario is a data path reinitialization that is triggered when the data path is in DataPathActivated. In this example, the Data Path State Machine transitions through every data path state as it makes the data path transmitter outputs quiescent, deinitializes the existing data path, initializes the new data path, and re-enables the transmitters. The module shall only set the Data Path State Complete flags once, when all chained state transitions have completed.

To facilitate understanding of this mechanism, this specification defines a variable called DataPathStateChangeFlagNeededV. This variable is for specification purposes only and is not reported in the memory map. The DataPathStateChangeFlagNeededV specification variable is per host lane and all lanes are initialized to 0 during the MgmtInit module state. This variable is updated in each transient data path state, depending on the advertised MaxDuration for that state. Once the final steady state in the chain is reached, if the DataPathStateChangeFlagNeededV variable is non-zero, the Data Path State Change Flag bit for that lane is set to 1.

6.3.2.1 Data Path control and status

A single register is provided for the host to control initialization and deinitialization of all data paths in a given bank. This register, called DataPathDeinit, is defined per host lane, to allow flexibility for a variety of data path configurations from a single memory map specification. When the host is requesting initialization or deinitialization of a data path, the host shall write the same value to all DataPathDeinit bits corresponding to all lanes in the applicable data path. The host may request initialization or deinitialization of multiple data paths with one TWI transaction.

The Data Path state register (Table 8-57) defines the current Data Path State for each data path in the module. The module reports the same Data Path State on all lanes in the data path. This synchronized state change behavior means the host only has to read the first lane of the data path to determine the data path state. Although the data path state machine behavioral model described in this specification describes a single state machine per data path, module software implementers may choose to write their software in a variety of ways and still meet the behavioral data path requirements. Some informative data path initialization flows are provided in Appendix B to facilitate understanding of the relationship between the initialization of physical structures in the module and data path-level reporting in the memory map.

6.3.2.2 DataPathDeactivated State

The DataPathDeactivated state is a steady state that indicates to the host that no data path is initialized on the indicated lane(s). The host may configure or reconfigure data paths on lanes that are reporting the DataPathDeactivated state in the Data Path State register (Table 8-57).

DataPathDeactivated is entered when any of the following conditions occur

a. The ResetS transition signal is TRUE (Table 6-8).
b. The module exits the Reset module state, for example on module insertion.
c. Any data path completes the DataPathDeinit state.

Upon entry into the DataPathDeactivated state, the module sets the Data Path state register (Table 8-57) for all lanes in the applicable data path(s) to DataPathDeactivated. If the exit conditions for DataPathDeactivated are not satisfied immediately on entry into the state, the module sets the Data Path State Change flag (Table 8-60) to 1 on each lane where the DataPathStateChangeFlagNeededV specification variable is non-zero before clearing DataPathStateChangeFlagNeededV for that lane. The module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag.

All transmitter outputs associated with the data path in DataPathDeactivated shall be quiescent throughout the state. Changes to Tx disable or squelch for data paths in DataPathDeactivated shall have no impact on the output quiescence of those data path.

Interrupt flag conformance in the DataPathDeactivated state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during DataPathDeactivated.

The Data Path State Machine shall only transition to DataPathInit when the DataPathDeinitS transition signal is FALSE (Table 6-15), unless the ResetS transition signal is TRUE (Table 6-8). The data path state shall remain in DataPathDeactivated as long as ResetS is TRUE. The Host shall provide a valid high-speed input signal at the required signaling rate and encoding type prior to the transition to DataPathInit. The host may request initialization of multiple data paths in one request.

6.3.2.3 DataPathInit State

The DataPathInit state is a transient state that indicates that the module is performing initialization activities on the data path. Initialization activities include application of the selected Application properties, application and/or adaptation of signal integrity settings, and optional power up of Tx and Rx data path electronics if opportunistic power savings was employed by the module in DataPathDeactivated. The host shall provide a valid high-speed input signal at the required signaling rate and encoding type prior to entering the DataPathInit state.

Upon entry into the DataPathInit state, the module sets the Data Path state register (Table 8-57) for all applicable lanes to DataPathInit. The module also ORs the current DataPathStateChangeFlagNeededV specification variable value for each lane in the data path with the advertised DataPathInit_MaxDuration value (Table 8-28). The advertised DataPathInit_MaxDuration includes the time to perform all of DataPathInit activities on all lanes in any data path or combination of multiple data paths for any supported Application. Host implementers should note that this maximum duration represents the worst-case elapsed time for the module to complete the DataPathInit state. If the DataPathInit_MaxDuration register is set to 0, the worst-case duration of DataPathInit is less than 1 ms and the module will not report the DataPathInit state in the Data Path State register and may not report the completion of the state via the Data Path State Changed flag or Interrupt signal.

Within the DataPathInit state, the module performs any remaining power-up activities for module electronics associated with the data path(s) in DataPathInit. In some cases, these electronics may be shared between multiple data paths. Depending on prior power up and down actions, some or all of these electronics may already be powered; in such cases, the power up sequence is bypassed. The details of the power up sequence are implementation-dependent and outside the scope of this specification.

During DataPathInit, the module shall also apply the selected Application properties in the Active Set (see section 6.2.3) to the applicable data path module resources. The details of how the module applies Application settings is implementation-dependent and outside the scope of this specification. The module shall also apply the signal integrity settings in the Active Set during DataPathInit. Entry into DataPathInit shall trigger a full initialization of all applicable data path(s). For example, attributes that require adaptation, such as CTLE settings, shall be adapted at the appropriate time during DataPathInit. The order in which signal integrity settings are applied and adapted is implementation-dependent and outside the scope of this specification. Implementers should note that no input signal may be present at the module Rx input at the time of initialization. In such cases, the module electronics shall be fully configured, such that any required adaptation or CDR locking occurs automatically at a later point in time when an input signal is provided, without host intervention.

For all data paths in DataPathInit, all Tx outputs shall be quiescent throughout the state. Changes to Tx disable or squelch for data paths in DataPathInit shall have no impact on the output quiescence of those data paths.

The host shall minimize TWI transactions while in this state. Dynamic memory map content may be unreliable while in this state and should not be read or written.

Interrupt flag conformance in the DataPathInit state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during DataPathInit. However, the module shall not clear any interrupt flags when exiting the DataPathInit state. Interrupt flags are only cleared when the host reads the flag.

If the DataPathDeinitS logic signal is TRUE at any time during DataPathInit, the data path state shall transition to DataPathDeinit. Otherwise, when the module has completed power-up and initialization of all Tx and Rx resources associated with the data path, and all applicable Tx and Rx flags, alarms, and warnings are valid, the data path state transitions to DataPathInitialized.

6.3.2.4 DataPathInitialized State

The DataPathInitialized state is a steady state. Data paths that are in the DataPathInitialized state are considered fully initialized. However, the output of one or more media lane transmitters whose data path is in DataPathInitialized is either squelched or disabled and so the data path is not ready to transmit live traffic.

Upon entry into the DataPathInitialized state, the module sets the Data Path state register (Table 8-57) for all lanes in the applicable data path(s) to the DataPathInitialized state. If the exit conditions for DataPathInitialized are not satisfied immediately on entry into the state, the module sets the Data Path State Change flag (Table 8-60) to 1 on each lane where the DataPathStateChangeFlagNeededV specification variable is non-zero before clearing DataPathStateChangeFlagNeededV for that lane. The module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag.

Interrupt flag conformance in the DataPathInitialized state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during DataPathInitialized.

Transmitter output quiescence for data paths in DataPathInitialized is determined per media lane by the setting in the Tx Disable and Tx Force Squelch controls, and the Tx LOS condition of the lane.

If the DataPathReDeinitS transition signal is TRUE at any time during DataPathInitialized, the data path state shall transition to DataPathDeinit. Otherwise, if the DataPathDeactivateS signal is FALSE at any time during DataPathInitialized, the data path state shall transition to DataPathTxTurnOn. Either of these conditions may be met upon entry into DataPathInitialized.

6.3.2.5 DataPathDeinit State

The DataPathDeinit state is a transient state where the module can deinitialize the resources associated with a data path. Deinitialization tasks are implementation dependent but can include tasks such as opportunistic power savings or module software variable clean-up.

DataPathDeinit is entered through either of the following host-initiated actions:

a. The DataPathDeinitS transition signal is TRUE (Table 6-15) while in the DataPathInit state.
b. The DataPathReDeinitS transition signal is TRUE (Table 6-16) while in the DataPathInitialized state.

Upon entry into the DataPathDeinit state, the module sets the Data Path state register (Table 8-57) for all lanes in the applicable data path(s) to the DataPathDeinit state. The module also ORs the current DataPathStateChangeFlagNeededV specification variable value for each lane in the data path with the advertised DataPathDeinit_MaxDuration value (Table 8-28). The advertised DataPathDeinit_MaxDuration, includes the time to perform all of DataPathDeinit activities on all lanes in any data path or combination of multiple data paths for any supported Application. Host implementers should note that this maximum duration represents the worst-case elapsed time for the module to complete the DataPathDeinit state. If the DataPathDeinit_MaxDuration register is set to 0, the worst-case duration of DataPathDeinit is less than 1 ms and the module will not report the DataPathDeinit state in the Data Path State register, nor report the completion of the state via the Data Path State Changed flag or Interrupt signal.

During DataPathDeinit, the module may power down applicable data path electronics for opportunistic power savings. In some cases, electronics may be shared with other data paths that are not in DataPathDeinit or DataPathDeactivated. In such cases, these electronics shall remain powered. Similarly, module implementers may identify certain electronics that require significant power up times. Module implementers may choose to keep these electronics powered even when the host requests data path deinitialization. If the host wants to ensure maximum power savings, the host should initiate a module transition to Low Power Mode by causing the LowPwrS signal to become TRUE.

For all data paths in DataPathDeinit, all Tx outputs shall be quiescent throughout the state. Changes to Tx disable or squelch for data paths in DataPathDeinit shall have no impact on the output quiescence of those data paths.

The host shall minimize TWI transactions while in this state. Dynamic memory map content may be unreliable for lanes in this state and should not be read or written.

Interrupt flag conformance in the DataPathDeinit state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during DataPathDeinit. However, the module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag or sends a reset signal.

When the module has completed deinitialization activities on all resources associated with the data path, the data path state shall transition to DataPathDeactivated.

6.3.2.6 DataPathTxTurnOn State

The DataPathTxTurnOn state is a transient state where the module enables the Tx output for all media lanes associated with the data path.

Upon entry into the DataPathTxTurnOn state, the module sets the Data Path state register (Table 8-57) for all lanes in the applicable data path(s) to the DataPathTxTurnOn state. The module also ORs the current DataPathStateChangeFlagNeededV specification variable value for each lane in the data path with the advertised DataPathTxTurnOn_MaxDuration value (Table 8-37). The advertised DataPathTxTurnOn_MaxDuration, includes the time to enable and stabilize the Tx output on all media lanes in any data path or combination of multiple data paths for any supported Application. Host implementers should note that this maximum duration represents the worst-case elapsed time for the module to complete the DataPathTxTurnOn state. If the DataPathTxTurnOn_MaxDuration register is set to 0, the worst-case duration of DataPathTxTurnOn is less than 1 ms and the module will not report the DataPathTxTurnOn state in the Data Path State register, nor report the completion of the state via the Data Path State Changed flag or Interrupt signal.

Interrupt flag conformance in the DataPathTxTurnOn state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during DataPathTxTurnOn. However, the module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag or sends a reset signal.

If the DataPathDeactivateS transition signal becomes TRUE at any time during DataPathTxTurnOn, the data path state transitions to DataPathTxTurnOff. The data path advances to DataPathActivated once all Tx outputs associated with the data path are enabled, have stabilized, and are ready to transmit live traffic.

6.3.2.7 DataPathActivated State

The DataPathActivated state is a steady state. Data paths that are in the DataPathActivated state are considered fully initialized and ready to transmit live traffic.

Upon entry into the DataPathActivated state, the module sets the Data Path state register (Table 8-57) for all lanes in the applicable data path(s) to the DataPathActivated state. If the exit conditions for DataPathActivated are not satisfied immediately on entry into the state, the module sets the Data Path State Change flag (Table 8-60) to 1 on each lane where the DataPathStateChangeFlagNeededV specification variable is non-zero before clearing DataPathStateChangeFlagNeededV for that lane. The module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag.

Interrupt flag conformance in the DataPathActivated state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during DataPathActivated.

All transmitter outputs associated with the data path in DataPathActivated shall be enabled throughout the state.

The data path state transitions to DataPathTxTurnOff if the host causes the DataPathDeactivateS transition signal to become TRUE for that data path. The host may transition multiple data paths to DataPathDeinit simultaneously.

One way for the DataPathDeactivateS transition signal to become TRUE is if the host sets the Apply_DataPathInit bits associated with the data path to 1. The host may choose to reconfigure one or more data paths while in DataPathActivated by applying a new Application in one of the Staged Control Sets to the applicable data paths using Apply_DataPathInit. The host shall set Apply_DataPathInit to a uniform value for all lanes in the data path being reinitialized. When Apply_DataPathInit bits are set to 1, the data path state will transition through the DataPathTxTurnOff -> DataPathInitialized -> DataPathDeinit -> DataPathDeactivated -> DataPathInit -> DataPathTxTurnOn -> DataPathActivated state sequence, reinitializing the new data path configuration in DataPathInit.
Prior to setting the Apply_DataPathInit bits for applicable lanes, the host shall provide a valid high-speed input signal at the required signaling rate and encoding type. Host implementers should note that the Apply_DataPathInit bits for all lanes in the data path shall be set with one TWI transaction. The host may request reinitialization of multiple data paths in the same TWI transaction. Module implementers should note that data paths excluded from the Apply_DataPathInit lane mask shall not transition Data Path States nor change data path properties. This selective control allows host reconfiguration of individual data paths in breakout Applications without affecting the operation of other data paths in the module.

The DataPathDeactivateS transition signal will also become TRUE if the host writes a 1 to the Tx Disable or Tx Force Squelch lanes associated with the data path during DataPathActivated or if one of those lanes experiences a Tx LOS event and Tx Squelch is supported and enabled.

6.3.2.8 DataPathTxTurnOff State

The DataPathTxTurnOff state is a transient state where the module performs the applicable Tx Disable and/or Tx Force Squelch action on applicable lanes in the data path. This state indicates to the host that the data path is no longer activated and cannot send traffic on all lanes.

Upon entry into the DataPathTxTurnOff state, the module sets the Data Path state register (Table 8-57) for all lanes in the applicable data path(s) to the DataPathTxTurnOff state. The module also ORs the current DataPathStateChangeFlagNeededV specification variable value for each lane in the data path with the advertised DataPathTxTurnOff_MaxDuration value (Table 8-37). The advertised DataPathTxTurnOff_MaxDuration, includes the time to enable and squelch or disable the Tx output on all media lanes in any data path or combination of multiple data paths for any supported Application. Host implementers should note that this maximum duration represents the worst-case elapsed time for the module to complete the DataPathTxTurnOff state. If the DataPathTxTurnOff_MaxDuration register is set to 0, the worst-case duration of DataPathTxTurnOff is less than 1 ms and the module will not report the DataPathTxTurnOff state in the Data Path State register, nor report the completion of the state via the Data Path State Changed flag or Interrupt signal.

Interrupt flag conformance in the DataPathTxTurnOff state is defined in section 6.3.3. All disallowed interrupt flags shall not be set during DataPathTxTurnOff. However, the module shall not clear any interrupt flags on the state change. Interrupt flags are only cleared when the host reads the flag or sends a reset signal.

Transmitter output quiescence for data paths in DataPathInitialized is determined per media lane by the setting in the Tx Disable and Tx Force Squelch controls, and the Tx LOS condition of the lane.

The data path advances to DataPathInitialized once the applicable Tx outputs associated with the Tx Enable or Tx Force Squelch action have achieved the requested behavior and have stabilized.

6.3.3 Interrupt Flag Conformance per State

Some flags are generated by the Module or Data Path State Machines, but the majority of flags are triggered by other sources. In some states, certain flags are not applicable and should be inhibited. The following sections define the conformance for all interrupts for each state in the Module and Data Path State Machines.

6.3.3.1 Module Flag Conformance per State

Table 6-19 describes the flag conformance for all module flags, per module state. In module states where a flag is indicated as 'Not Allowed', the module shall not set the associated flag bit while the module is in that state. All module flags shall be 'Not Allowed' throughout the Resetting, Reset, and MgmtInit states. Module flag conformance is not dependent on Data Path State. Some module interrupts are module-configurable; Table 6-19 defines the flag conformance for each configuration option for those flags. Host implementers should note that if certain interrupts are undesirable, the host may mask those interrupts by setting the corresponding interrupt mask bit at any time after the management interface is initialized.

Table 6-19 Module Flag Conformance

Flag	Page	Byte	ModuleLowPwr Fault	ModulePwrUp ModulePwrDn ModuleReady
Module state change	00h	8	Allowed	Allowed
Module temperature	00h	9	Allowed	Allowed
Vcc 3.3V	00h	9	Allowed	Allowed
Aux1 – TEC Current	00h	10	Not Allowed	Allowed
Aux2 – TEC temp	00h	10	Not Allowed	Allowed
Aux2 – Laser temp	00h	10	Not Allowed	Allowed
Aux3 – Laser temp	00h	11	Not Allowed	Allowed
Aux3 – addl voltage	00h	11	Allowed	Allowed
Vendor-defined	00h	11	See below	Allowed

The vendor-defined flag is Allowed in ModuleLowPwr if and only if it applies to a feature that is available in Low Power Mode.

6.3.3.2 Lane-Specific Flag Conformance per State

Table 6-20 and Table 6-21 describe the flag conformance for all lane-specific flags, per Data Path State. In Data Path States where a flag is indicated as 'Not Allowed', the module shall not set the associated flag bit while the data path is in that state. All lane-specific flags shall be 'Not Allowed' throughout the Reset and MgmtInit module states. For all other module states, implementers should refer to the Data Path State to determine lane-specific flag conformance. Host implementers should note that if certain interrupts are undesirable, the host may mask those interrupts by setting the corresponding interrupt mask bit at any time after the management interface is initialized.

Table 6-20 Lane-Specific Flag Conformance

Flag	Page	Byte	DataPath Deactivated	DataPath Initialized	DataPathInit	DataPathDeinit
Data Path State Change[1]	11h	134	Allowed	Allowed	Not Allowed	Not Allowed
Tx Fault	11h	135	Allowed	Allowed	Allowed	Allowed
Tx LOS	11h	136	Not Allowed	Allowed	Not Allowed	Not Allowed
Tx CDR LOL	11h	137	Not Allowed	Allowed	Not Allowed	Not Allowed
Tx Adaptive Input Eq Fail	11h	138	Not Allowed	Allowed	Allowed	Not Allowed
Tx output power High Alarm	11h	139	Allowed	Allowed	Allowed	Allowed
Tx output power Low Alarm	11h	140	Not Allowed	Allowed	Not Allowed	Not Allowed
Tx output power High Warning	11h	141	Allowed	Allowed	Allowed	Allowed
Tx output power Low Warning	11h	142	Not Allowed	Allowed	Not Allowed	Not Allowed
Tx Bias High Alarm	11h	143	Allowed	Allowed	Allowed	Allowed
Tx Bias Low Alarm	11h	144	Not Allowed	Allowed	Not Allowed	Not Allowed
Tx Bias High Warning	11h	145	Allowed	Allowed	Allowed	Allowed
Tx Bias Low Warning	11h	146	Not Allowed	Allowed	Not Allowed	Not Allowed
Rx LOS	11h	147	Allowed	Allowed	Allowed	Allowed
Rx CDR LOL	11h	148	Not Allowed	Allowed	Not Allowed	Not Allowed
Rx Input Pwr High Alarm	11h	149	Allowed	Allowed	Allowed	Allowed
Rx Input Power Low Alarm	11h	150	Not Allowed	Allowed	Not Allowed	Not Allowed
Rx Input Power High Warning	11h	151	Allowed	Allowed	Allowed	Allowed
Rx Input Power Low Warning	11h	152	Not Allowed	Allowed	Not Allowed	Not Allowed

Note 1: The Data Path State Changed flag is only allowed when the DataPathStateChangeFlagNeededV specification variable is nonzero and the exit conditions for the applicable steady state are not satisfied when the state is entered.

Table 6-21 Lane-Specific Flag Conformance, additional data path states

Flag	Page	Byte	DataPath Activated	DataPath TxTurnOn	DataPath TxTurnOff
Data Path State Change[1]	11h	134	Allowed	Not Allowed	Not Allowed
Tx Fault	11h	135	Allowed	Allowed	Allowed
Tx LOS	11h	136	Allowed	Allowed	Allowed
Tx CDR LOL	11h	137	Allowed	Allowed	Allowed
Tx Adaptive Input Eq Fail	11h	138	Allowed	Allowed	Allowed
Tx output power High Alarm	11h	139	Allowed	Allowed	Allowed
Tx output power Low Alarm	11h	140	Allowed	Allowed	Allowed
Tx output power High Warning	11h	141	Allowed	Allowed	Allowed
Tx output power Low Warning	11h	142	Allowed	Allowed	Allowed
Tx Bias High Alarm	11h	143	Allowed	Allowed	Allowed
Tx Bias Low Alarm	11h	144	Allowed	Allowed	Allowed
Tx Bias High Warning	11h	145	Allowed	Allowed	Allowed
Tx Bias Low Warning	11h	146	Allowed	Allowed	Allowed
Rx LOS	11h	147	Allowed	Allowed	Allowed
Rx CDR LOL	11h	148	Allowed	Allowed	Allowed
Rx Input Pwr High Alarm	11h	149	Allowed	Allowed	Allowed
Rx Input Power Low Alarm	11h	150	Allowed	Allowed	Allowed
Rx Input Power High Warning	11h	151	Allowed	Allowed	Allowed
Rx Input Power Low Warning	11h	152	Allowed	Allowed	Allowed

Note 1: The Data Path State Changed flag is only allowed when the DataPathStateChangeFlagNeededV specification variable is nonzero and the exit conditions for the applicable steady state are not satisfied when the state is entered.

7 Advanced Management Features

The features described in this section provide advanced control and status and are optional. Support for each of these features is advertised in the module memory map.

7.1 Versatile Diagnostics Monitoring (VDM)

Versatile diagnostics monitoring (VDM) is defined as a versatile mechanism to extend the number of parameters, by up to 256 parameters that can be monitored and alarmed per bank; in addition to the monitors and alarms already defined in Lower Memory and Pages 11h. The use of the Bank Register R126 is identical to Pages 10-1Fh to extend the lane count for modules with greater than 8 lanes.

7.1.1 Overview

Advanced and more complex transceiver modules may need to be able to monitor an extended parameter list as well as to generate alarms on these parameters. To allow monitoring of these parameters pages 20-2Fh in the CMIS MSA memory space are utilized. The basic monitoring techniques are the same as for other monitored parameters (i.e., they support current value, latched warning/alarm status, masks and thresholds). Page 01h, Byte 142 Bit 6 is used to indicate to the host device that pages 20h-2Fh are supported by the module. Page 2Fh provides more detailed advertising.

For a module implementing a Dense Wavelength Division Multiplexing optical interface, there is a significant benefit in providing access to additional diagnostic monitoring parameters specifically for a DWDM module. In DWDM the wavelength or frequency of the laser is an extremely important parameter and monitoring it allows the health of the laser to be known. When a direct measurement of the error in the frequency is not available, the laser temperature deviation from target is often used as a proxy. In addition, DWDM modules typically use a thermo-electric cooler (TEC) to control the laser temperature. The current flowing through the TEC is a strong indicator of the health of the module. A warning or error indication in any of these parameters can be an early indication of pending module failure.

The details of the additional parameters that can be supported are listed in Table 8-99 which includes specific support for PAM4 modulation and optical transmission wavelengths on DWDM grid. For a PAM4 signal several additional parameters are very useful to determine the health of the module and the line environment. These include bit error ratio and frame error rate calculations, a signal-to-noise ratio measurement and a level transition measurement that characterize the PAM eye. The support of VDM is an optional feature accessible through pages 20h-2Fh, summary as shown in Table 8-95.

If supported, VDM is defined by:

- Pages 20h-23h: Configures a specific DDM for each parameter id.
- Pages 24h-27h: If configured will return the real-time value (current value) for the configured VDM parameter.
- Pages 28h-2Bh: Thresholds Identifier 1 to 64 that is used to generate an Alarm or Warning.
- Page 2Ch: Up to 256 COR latched alarms, 4 bits per alarm.
- Page 2Dh: Up to 256 Mask Bits for the respective alarms.
- Page 2Fh: Additional control register and advertisement register.
- Banks 0-3h: Extends the number of lanes supported using the bank registers.

A single bit is used to advertise if pages 20-2Fh are supported and then the host may read additional registers for additional configuration specific to VDM.

It is expected that not all possible features will be supported by all modules or on all lanes. To address this situation, this specification allows the module to advertise which parameters are being monitored. Some parameters may be module-level in scope, some may be related to a data path, and some may be lane-specific. This information is conveyed by the module to the host in the 2-byte configuration register for each parameter monitored. To indicate that one or more parameters are not supported the module will report 00h in both bytes of the configuration register for that parameter.

Up to 256 different parameters can be monitored per bank, each providing a real-time value as well as alarm and warning flags. 64 threshold value sets are provided, and each of the 256 parameters is associated by the module with one of the threshold value sets from a threshold group. The parameter configuration registers indicate which threshold group and threshold number set is to be used with each parameter. Note that this implies that multiple parameters may share the same threshold set (for example, if the same parameter is measured on multiple lanes).
The 256 parameters are spilt into 4 groups. Each group consists of one page of configuration, one page of real-time values, one page of thresholds and ¼ page each of alarms and masks.

To facilitate future functionality without major specification changes, the parameter configuration registers provide a coded value for the specific parameter to be monitored.

7.1.2 PAM4 Monitored Parameters

Figure 7-4 below shows a general block diagram of the optical ingress path of a module showing the location where the SNR and level transition parameters are measured.

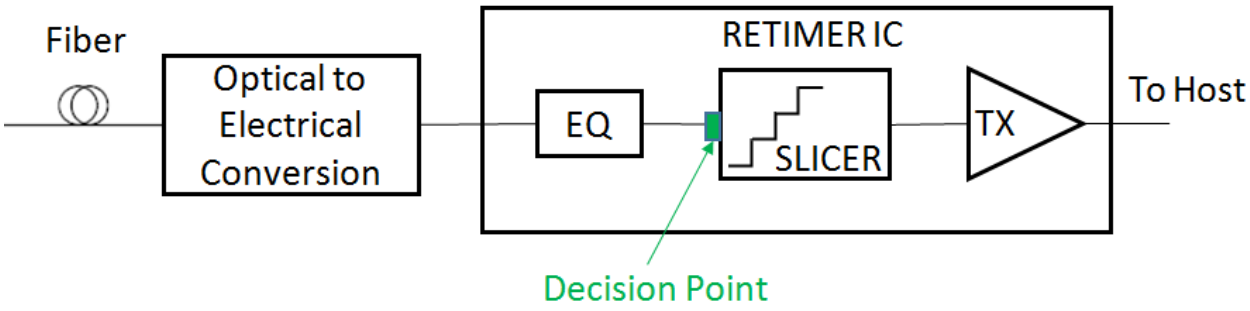


Figure 7-1: Optical ingress path of Module

Figure 7-2is a view of the aggregate PAM4 data expressed as a histogram measured at a vertical slice in the center of the eye, showing the measurement method for SNR and level transition parameters.

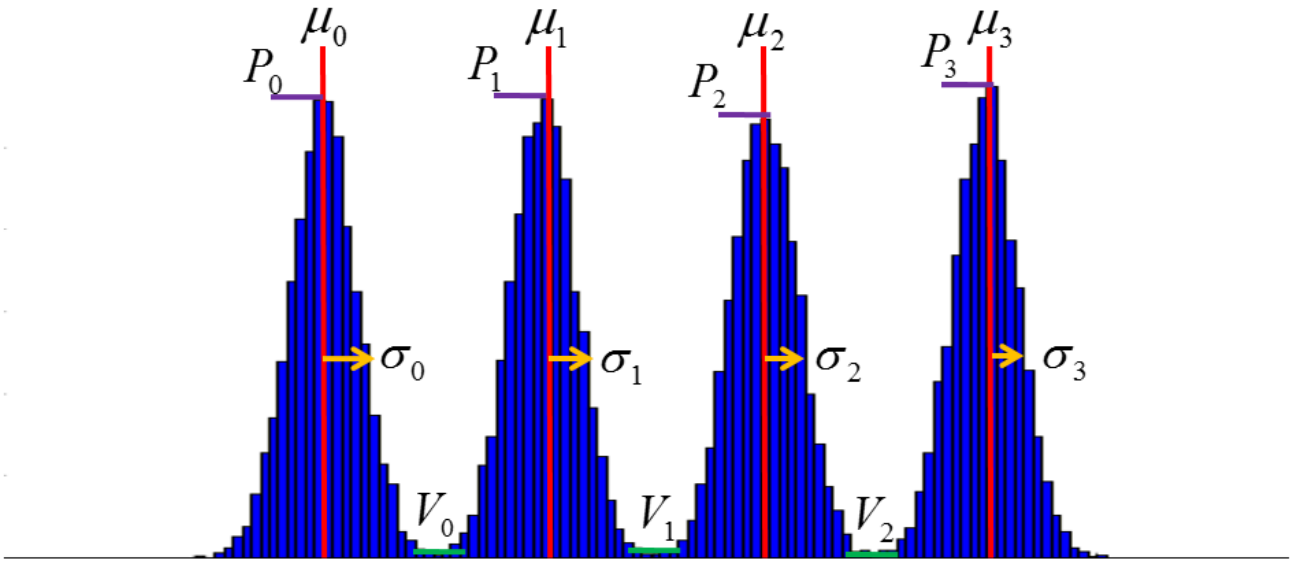


Figure 7-2: PAM4 vertical slice histogram

The histogram x-axis is in bins and the y-axis is in number of bin hits. The number of bins and the hit count magnitude is vendor specific. The histogram is taken at the point in the time domain where data is converted from analog to digital. The PAM4 slicer determines the best points to split the data between values of 0, 1, 2 or 3. The peak is the bin with the largest number of counts between any two valleys (or below valley 1/above valley 3 for the first and last peaks). The valley location is determined by the slicer, and is the bin number where data below is considered to be i and data above is considered to be i+1.

The calculations for the reported eye parameters are:

SNR = 10* $\log_{10}(\min\{SNR_0, SNR_1, SNR_2\})$ where $SNR_i = (\mu_{i+1} - \mu_i)/(\sigma_{i+1} + \sigma_i)$, expressed in 1/256 dB units

LTP = 10* $\log_{10}(\min\{LTP_0, LTP_1, LTP_2\})$ where $LTP_i = (P_{i+1} + P_i)/(2V_i)$, expressed in 1/256 dB units

Where,

μ_i: level of ith peak, optionally averaged over neighboring bins

σ_i: std dev of ith peak, optionally averaged over neighboring bins

P_i: height of ith peak, optionally averaged over neighboring bins

V_i: height of ith valley, optionally averaged over neighboring bins

For the vendor specified wavelength, the accuracy of the reported SNR and LTP parameters shall be better than +/-3 dB over specified temperature and voltage.

7.1.2.1 SNR

This feature measures the electrical signal-to-noise ratio on the ingress optical lane, as defined in section 8.10.3. It is the minimum of the individual eye SNR values, where the SNRi for each of the three eyes is defined as the ratio of the difference of the mean voltage between neighboring levels divided by the sum of the standard deviations of the two neighboring levels.

SNR is encoded as a 16-bit unsigned integer in units of 1/256 dB. For example, a value of 1380h will be interpreted as an SNR of 19.5 dB.

7.1.2.2 PAM Level Transition Parameter

This feature measures the electrical level slicer noise, as defined in section 8.10.3. It is the minimum of the individual PAM level LTP values, where the LTP for each PAM level is defined as the average of the peak histogram intensity of neighboring PAM levels divided by the minimum histogram intensity between them. Both the SNR and LTP parameters measure signal-to-noise but the LTP parameter is more sensitive to a noise floor.

PAM Level Transition Parameter is encoded as a 16-bit unsigned integer in units of 1/256 dB. For example, a value of 3080h will be interpreted as an LTP of 48.5 dB. It is possible that the minimum histogram intensity between PAM levels is actually zero in which case this parameter would be infinite. In this case the special value of FFFFh will be used. If the parameter measures a value of greater than 255.996 dB but is not infinite, then FFFEh will be used.

7.1.2.3 Error Metrics

Frame error rate is reported in RS(544,514) FEC equivalent frames (see IEEE 802.3 Clause 91.5). If the actual FEC is not RS(544,514) then the measured frame error rate is converted. So for example, if the FEC frame size is 10% larger than the RS(544,514) FEC frame, then the reported frame error rate will be 10% higher than the measured frame error rate. This is done so as to be able to compare frame error rates regardless of the FEC encoding employed.

Two different error metrics may be supported:

- RS(544,514) Frame Error Count (FERC): This extensive parameter measures the number of uncorrected/errored RS(544,514) equivalent frames
- Pre-FEC Bit Error Ratio (BER): This intensive parameter is the total number of errored bits that were corrected by the FEC during an interval divided by the total number of bits received in that interval. *Note that different FEC schemes will have different maximum pre-FEC BER requirements for a specific corrected BER maximum target.*

Both BER and FERC will be monitored using the following technique:

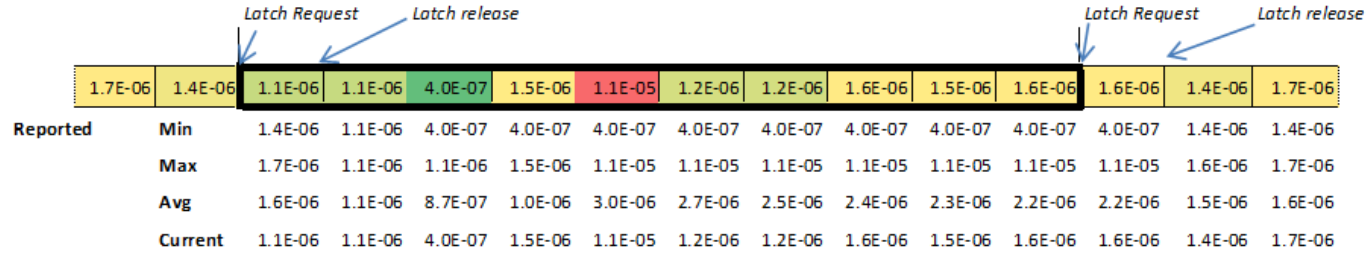


Figure 7-3: Error rate accumulation intervals

The module shall collect BER/FERC data over a vendor-specific fine time slice, defined by the module (for example, 1 ms). The host may read the data at a slower rate.

The module calculates a BER/FERC at each fine interval (light borders). The Host may have performance monitoring intervals (dark borders). Figure 7-3 shows a series (in time) of fine intervals punctuated by counter latch events that demark the host monitoring interval. If supported by the module, the host can read various calculated values. The selection of which value(s) is/are available depends on the parameter type identifier.

Current:
If supported, the module shall keep a recent reading for the host to read at any time. This is also referred to as the “instantaneous” value.

Latched Average:
If supported by the module, the average value shall be determined by using the counters reset function to program the time interval of interest. The module shall report a continuously averaged reading over the entire previous interval. The host sets the Latch Average Counters bit to indicate to the module to end the previous interval and start a new one. The module will immediately (within tNACK) clear to zero the Average Latch Done bit, and then set it to 1 when the data is ready for reading. The module will continue to accumulate data into an averaging circuit even while the Latch Average Counters bit is set, but will not update the real-time parameter value until the Latch Average Counters bit is cleared. When the Latch Average Counters bit is cleared, and then set again, the new interval data will be latched by the module. In this way, no data will be lost and the host can be assured that data is not changing while it’s being read.

Latched Minimum:
If supported by the module, the minimum value shall be determined by using the counters reset function to program the time interval of interest. The module shall report the minimal fine-interval reading collected over the entire previous host monitoring interval. The host sets the Latch Minimum Counters bit to indicate to the module to end the previous interval and start a new one. The module will immediately (within tNACK) clear to zero the Minimum Latch Done bit, and then set it to 1 when the data is ready for reading. The module will continue to accumulate data into a minimizing circuit even while the Latch Minimum Counters bit is set, but will not update the real-time parameter value until the Latch Minimum Counters bit is cleared. When the Latch Minimum Counters bit is cleared, and then set again, the new interval data will be latched by the module. In this way, no data will be lost and the host can be assured that data is not changing while it's being read.

Latched Maximum:
If supported by the module, the maximum value shall be determined by using the counters reset function to program the time interval of interest. The module shall report the maximal fine-interval reading collected over the entire previous host monitoring interval. The host sets the Latch Maximum Counters bit to indicate to the module to end the previous interval and start a new one. The module will immediately (within tNACK) clear to zero the Maximum Latch Done bit, and then set it to 1 when the data is ready for reading. The module will continue to accumulate data into a maximizing circuit even while the Latch Maximum Counters bit is set, but will not update the real-time parameter value until the Latch Maximum Counters bit is cleared. When the Latch Maximum Counters bit is cleared, and then set again, the new interval data will be latched by the module. In this way, no data will be lost and the host can be assured that data is not changing while it's being read.

Note that the thresholds system is maintained for BER and FERC, but the low thresholds should be 0, and the high threshold for FERC should also be 0 unless other error correcting schemes are present.

7.1.3 DWDM Monitored Parameters

7.1.3.1 TEC Current

If supported, this parameter monitors the amount of current flowing to the TC of a cooled laser. A single parameter for a whole-module TC is available in the Auxiliary monitoring capabilities. Modules should use the Versatile VDM system to provide for a per-lane TEC controller. See Table 8-99 for encoding, units and scaling information.

7.1.3.2 Laser Frequency

If supported, this parameter monitors the difference (in frequency units) between the target center frequency and the actual current center frequency. It is a similar measurement to the Laser Temperature except expressed as a frequency difference instead of a temperature difference, and vendors may support one or the other measurement, or both. See Table 8-99 for encoding, units and scaling information

7.1.3.3 Laser Temperature

If supported, this parameter monitors the laser temperature difference between the target laser temperature for a cooled laser, and the actual current temperature. It is a similar measurement to the Frequency Error except expressed as a temperature difference instead of a frequency difference, and vendors may support one or the other measurement, or both. A single parameter for a whole-module laser frequency is available in the Auxiliary monitoring capabilities. Modules should use the Versatile VDM system to provide for a per-lane laser temperature. See Table 8-99 for encoding, units and scaling information.

7.2 Command Data Block (CDB) Message Communication

The module advertises support for CDB using the fields on Page 01h described in section 8.4.11.
The definition for CDB command fields on page 9Fh can be found in section 8.12.
Pages A0h-AFh contain up to 2048 bytes of extended payload (EPL).
Details regarding the number of EPL pages can be found in section 8.13.

CDB reads and writes are performed on memory map pages 9Fh-AFh. Page 9Fh is used to specify the CDB command to be executed and also provides an area for a local payload (LPL) of up to 120 bytes. The execution status of the CDB command specified during a write operation to page 9Fh can be read in bytes 37 and 38 the Lower Memory. See section 8.2.7 for details. When a CDB command has completed, the module notifies the host using the maskable interrupt flag in byte 8 on the Lower Memory (see Table 8-5).

7.2.1 CDB support levels

If CDB is supported and whenever a CDB command is received, the actions that the module may take can be broken down into the following steps.

1. Capture the CMD code and payload (into a buffer or queue)
2. Perform a CdbCheckCode verification.
3. Validate that the CMD Code and its parameters are valid.
4. Validate that the CMD Code can be executed in the current module state or user privilege level.
5. Return error codes to status register or schedule command for execution.
6. Execute the command
7. Complete execution of command and validate if command has execution errors or was successful.
8. Compile return data of the CDB command into a response buffer and response CDB message memory map.
9. Write error codes or success codes to the status register and set byte 8 CDB block complete bit to 1. As a consequence, the IntL signal will be asserted if the signal is not masked.

The steps described above may vary by module vendor but the overall behavior of the CDB is identical. (i.e. a CDB command sent will result in a CDB response). A module not responding to a CDB command is considered faulty and the host may need to perform a hardware RESET or issue a CMD ABORT to restore the module CDB functions.

Module vendors may choose to support CDB at varying levels based on the processing capabilities of its management interface. These options are:

- CDB processing
    - in background (NACK until command captured but not processed) or
    - in foreground (NACK until command completes execution)
- Number of CDB instances supported (1 or 2)

Note: Modules supporting CDB processing in background typically require a more powerful CPU as well as more memory resources such as NVR or RAM. Modules supporting CDB processing in foreground keep CPU resources to a minimum to be cost effective or to minimize power consumption of the system.

This CMIS defines the support of up to two CDB blocks in foreground or background. When two CDB instances are supported in background, this means that there could be up to two CDB operations running in parallel, processing or executing in background at the same time. This is in addition to the TWI access of the memory mapped registers at the same time. When CDB operations are running in foreground, see section 7.2.1.1, the TWI interface will NACK until the CDB command completes it execution. A module that supports 2 CDB instances in the foreground will only be able to run one CDB command at a time which may be triggered by using bank 0 or 1. Each CDB block requires a bank. See Figure 8-1Figure 8-1. CDB Block 1 resides in Bank 0 and CDB Block 2 resides in Bank 1.

7.2.1.1 Sequential CDB (foreground only)

A module may implement CDB message handling in foreground mode only. This is indicated by setting Page 01h Byte 163 Bit 5 to 0b. This means that the module will NACK after the TWI write transaction to page 9Fh CDB command register and continue to NACK until the requested CDB command execution has completed. While command execution is in progress, any read or write access to TWI bus will NACK. For example, trying to read the CDB status register 37 or 38 will return a NACK. Once the command has completed execution, the module shall set the CDB status register 37 or 38 (for bank 0 and 1) respectively and start responding to TWI commands. A host shall implement NACK handling and retries for these types of modules when using CDB.

In these modules, while CDB operation is in progress, all other accesses to memory mapped registers will not be available. In the event that the module has a bug and NACKs forever, the host will need to reset the module via the RESETn pin or toggle the power supply to the module.

7.2.1.2 One CDB with parallel register access (background mode)

A module may advertise that it implements only one CDB instance in background mode. This is indicated by setting Page 01h Byte 163 Bits 7-6 as 01b and Bit 5 to 1b. In this mode, after the TWI write transaction to page 9Fh CDB command register the module will NACK only for a very short time simply indicating that the command is captured but have not yet being processed. The TWI bus will start responding once the command is captured. Since only one CDB is implemented, the module will only respond to CDB commands in Bank 0. Reading the CDB 0 status register Byte 37 will return the status Bit 7 set to 1b (STS_BUSY=1). The host shall not attempt to send another CDB command until the CDB operation is completed indicated by reading Byte 37 and waiting for STS_BUSY=0b. (See Table 8-10). If the host attempts to send another CDB command while the CDB instance is busy (indicated by the STS_BUSY status bit) the command may be ignored or the command may be processed if STS_BUSY is cleared in background during the TWI transaction time. This makes the behavior of the CDB command or response unpredictable. The only CDB command that is allowed when the CDB status is indicating STS_BUSY, is the CDB General ABORT 0004h message, which is designed to ABORT a command that has not completed within expected command execution time and clear the STS_BUSY bit by aborting the command.

The status register (Byte 8, bit 6 (L-CDB block 1 command complete)) when set to 1 and not masked by its associated mask bit (Byte 31, bit 6) will generate an IntL signal.
These types of modules may support firmware upgrades using CDB while the module is running. Depending on the implementation of the host firmware, the module may also support running Performance Monitors (PM) at the same time, but it is up to the host to manage the one instance of CDB for different applications at the same time.

7.2.1.3 Two CDB instances with parallel register access (background mode)

A module having two CDB instances in background is simply an extension of a module having one CDB instance in background. Here the module can now run two simultaneous CDB commands in background. The same rules regarding STS_BUSY apply for the respective CDB instance, where the host shall not send another CDB command unless the STS_BUSY bit is cleared (with the exception of the General ABORT CMD 0004h). Byte 8, bits 7 - 6 (CDB block command complete bits), when set to 1 and not masked by its associated mask bit (Byte 31, bits 7--6) will generate an IntL signal. In all cases, if an existing command is still in execution (STS_BUSY = 1), module shall reject additional CDB commands and protect the content of CDB not to be overwritten.

These types of modules allow the host to have a separate thread or task, for example, having one thread specifically for firmware upgrades only and another thread for performance monitoring, diagnostics and other features.

Note that in order to have multiple threads, the host must implement proper bank and page registers and TWI writes/reads interlocks. This is one of the main reasons that the status registers 37 and 38 have been located in Lower Memory where these registers are always available.

There should be no differences between CDB commands supported by each instance. Both CDB instances shall support the same CDB commands advertised.

7.2.2 Firmware Upgrade Commands in CDB.

The CDB commands detailed in section 9.6 defines commands but not the procedure to perform a firmware upgrade. This section details the common procedure to upgrade the firmware on the module. Figure 7-4 defines the flow chart for upgrading the firmware of a module while Figure 7-5 defines the flow chart for reading back the complete firmware blocks. Reading back the complete firmware block is an optional feature that may be supported by some modules only.

If firmware upgrade is implemented, the module vendor provides a file for upgrading the firmware of a module and a separate optional file for reading back the firmware. The module advertises the number of bytes of "Start command payload size" in Page 9F Byte 138 CMD 0041h corresponding to the number of bytes at the beginning of the firmware upgrade file. The file may be in binary or ASCII, for example Intel hex file format. If the file is in ASCII, it is assumed that the file is to be decoded into a contiguous block of memory by the host.

If the module advertises that Write LPL or EPL is not supported then the module may not be able to download firmware using this CDB mechanism, but the module may still be able to query firmware information using the CDB CMD 0100h.

7.2.2.1 Firmware Upgrade using CDB

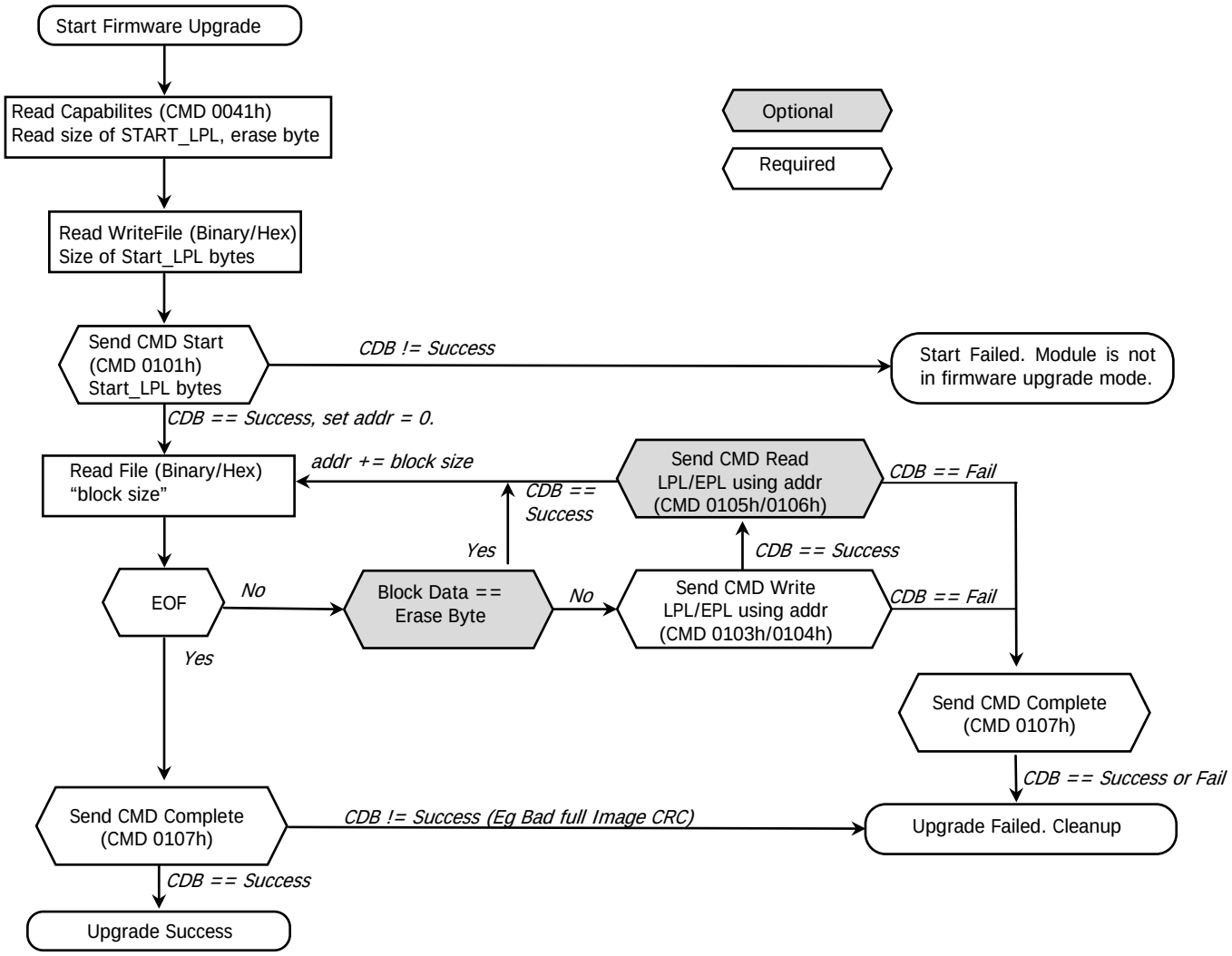


Figure 7-4: Firmware Upgrade using CDB

Firmware upgrade starts by the host reading the capabilities of the module using CBD CMD 0041h. The host reads the vendor file into contiguous addressable binary bytes defined as the download image.

To start the upgrade, the host is expected to read the first number of "Start Command Payload Size" bytes from the download image and send these bytes as part of the CDB CMD 0101h (Start Download) LPL payload. Assuming that the CDB CMD 0101h operation is successful, the host shall set an "addr" variable to 0. This is the address "addr" variable that will be sent in subsequent Write LPL/EPL or Read LPL/EPL commands. Once the CMD 0101h is successful, the module is in a state ready to accept data from the host using the advertised method which could be either Write LPL or Write EPL.

The next group of operations send the data to the module by reading subsequent bytes of the download image in blocks smaller than or matching the size of the Write LPL or EPL commands, then sending it using CMD 0103h or 0104h. In Figure 7-4 there are two optional blocks shown. The first optional block is introduced to speed up the firmware upgrade process by not even sending blocks of data matching the erased state. The second optional block slows down the firmware download process by allowing the most recently sent block to be read back, and is only recommended in debug mode.

Downloading data to the module in the firmware upgrade process ends when the host has sent all the data from the download image and no errors have occurred in all the messaging. The host then completes the firmware upgrade by sending the CMD Complete 0107h. This will trigger the module to perform any appropriate validation. If the validation fails, this command may cause the CDB status to return a failure code. The host should not assume that all modules will perform a full validation.

In the event of an error during Write/Read LPL or EPL commands, the host shall also send a CMD Complete. The module firmware may use this message to stop the current firmware upgrade sequence. A new sequence may be restarted to retry upgrading the firmware in the module again. The host may send a CDB CMD Abort (0102h) at any time during the transfer to abort the firmware upgrade, if the module advertises that the abort command is supported.

7.2.2.2 Firmware Readback using CDB

Reading back the complete image block may be achieved using the flow chart shown in Figure 7-5.

In order to allow a full image readback feature, the module vendor shall provide a different file called the readback file. The file shall have the same number of bytes in the "Start Command Payload Size" bytes. Within these bytes, the vendor shall have a field denoting that the operation is a readback, in which case, the CMD 0101h that starts the download does not perform an image erasure.

It is worthwhile to mention here that most module vendors may not support reading back the complete image from the module. If readback is supported, a file may be generated from the readback data such that the data of the file matches that of the download file used. At least one byte or bit will be different as the header of the readback and download files are different.

To start the readback, the host is expected to read the first number of "Start Command Payload Size" bytes from the readback image and send these bytes as part of the CDB CMD 0101h (Start Download) LPL payload. Assuming that the CDB CMD 0101h operation is successful, the host shall set an "addr" variable to 0. This is the address "addr" variable that will be sent in subsequent Read LPL/EPL or Read LPL/EPL commands. Once the CMD 0101h is successful, the module is in a state ready to return data to the host using the advertised method which could be either Read LPL or Read EPL. The number of bytes to readback as shown in Figure 7-5 will be the size of this readback file. The data content of the readback file past the first "Start Command Payload Size" bytes will not be sent to the module.

At the completion of the readback feature, the host shall send a CMD Complete (0107h) command to tell the module that the set of operations is over. The module may simply set a flag such that subsequent Read LPL or EPL commands returns nothing or an appropriate error code. Similarly on errors the same CMD Complete (0107h) is sent.

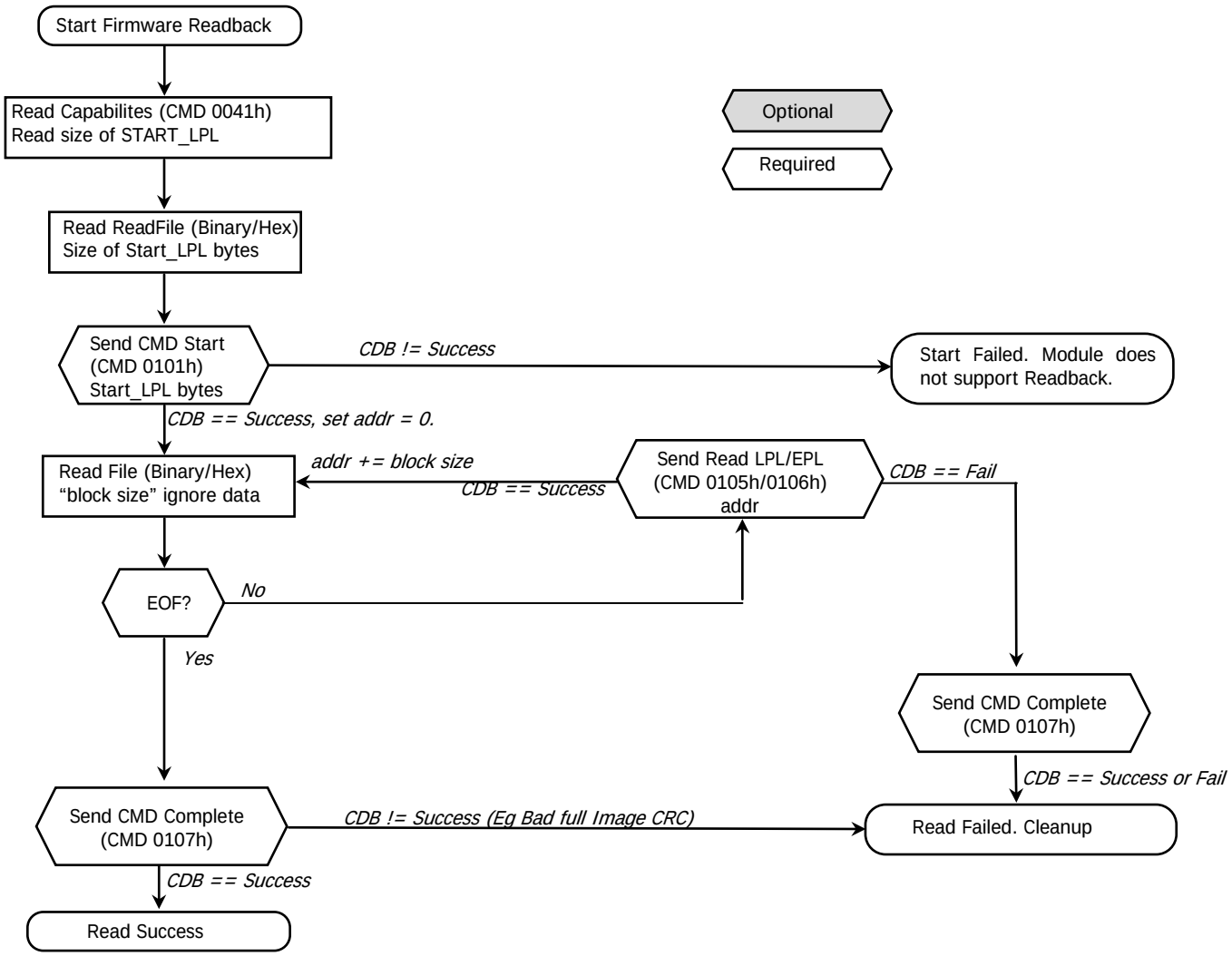


Figure 7-5 Firmware Image Readback using CDB

7.2.3 Performance Monitoring using CDB.

CDB implementation of performance monitoring returns diagnostics data such as minimum, average, maximum and current values of monitored parameters. A module may advertise the list of supported performance monitoring commands using the CDB CMD 0042h (see section 9.3.3). CDB for performance monitoring allows the host to read a large number of parameters using a single CDB transaction, however autonomous alarms are not reportable using CDB. If autonomous alarms are required, then the Versatile Diagnostics Monitoring implemented in Pages 20h-2Fh should be used.

CDB and Versatile Diagnostics Monitoring may be both implemented within the same module. Since both methods return minimum, average and maximum values, these statistics may be tracked independently or synchronously. When both methods are implemented, the tracking mode defaults to independent tracking and a CDB command may be used to change the mode to synchronous tracking (linked mode).

Whenever the module restarts (including Run Image A/B command), the performance monitoring mode reverts to independent tracking of the minimum, average and maximum values of all the parameters that it advertises. This means that the minimum, average and maximum values read using CDB and read using Pages 20h-2Fh differ because the time and duration of these latching parameters are not synchronized. The clearing and resetting of latches between CDB and Page 2Fh will be completely independent, and the module maintains two separate internal data for these minimum, average and maximum values.

Once the system has started, the host may change the CDB performance monitoring mode using CMD 0200h into a synchronous linked mode. When changing modes, it is assumed that all latches are cleared and reset with a mode change. In the linked mode, the module is expected to maintain one common minimum, average and maximum value and shall return the same information whether the messaging interface is via CDB or Page 20h-2Fh. Furthermore in a linked mode a latched will be cleared whether it is cleared by a CDB command or by a write to register in Page 2Fh.

In both performance monitoring methods using either Versatile Diagnostic Monitoring or CDB, the time at which the module starts collecting performance monitoring data or method or internal time granularity at which these data are processed remains undefined. It is assumed that the host will setup the datapaths and after the datapaths are valid, the host will read and discard the first set of minimum, average and maximum values and restart the latching. This is because the first set of data may consist of transient data where the minimum, average and maximum values may reflect transients in the system. In both performance monitoring methods using either Versatile Diagnostic Monitoring or CDB, the time at which the module starts collecting performance monitoring data or method or internal time granularity at which these data are processed is defined by the vendor. The module will follow section 6.3.3 for interrupt compliance. The host, upon establishing that the operational conditions are satisfactory for the data of interest, should read and discard the first set of minimum, average and maximum values and restart the latching. This is because this first set of data may consist of transient data where the minimum, average and maximum values may reflect transients in the system or non-operational conditions.

7.3 Module Boot Record (MBR)

Reserved for future activity

8 Module Management Memory Map

This section defines the register memory map for a CMIS compliant module.

8.1 Overview

8.1.1 Memory Structure and Mapping

The TWI protocol defined in section 5.2 only supports eight-bit addresses. This limits the management memory that can be directly accessed by the host to 256 bytes, which is divided in **Lower Memory** (addresses 00h through 7Fh) and **Upper Memory** (addresses 80h through FFh).

A larger addressable management memory is required for all but the most basic modules. This is supported by a structure of 128-byte pages, together with a mechanism for dynamically mapping any of the 128-byte pages from a larger internal management memory space into Upper Memory the host addressable space.

The addressing structure of the additional internal management memory[2] is shown in Figure 8-2. The management memory inside the module is arranged as a unique and always host accessible address space of 128 bytes (Lower Memory) and as multiple upper address subspaces of 128 bytes each (**Pages**), only one of which is selected as host visible in Upper Memory. A second level of Page selection is possible for Pages for which several instances exist (e.g. where a **bank** of pages with the same Page number exists).

This structure supports a flat 256 byte memory for passive copper modules and permits timely access to addresses in the Lower Memory, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function in the Lower Page. For more complex modules which require a larger amount of management memory the host needs to use dynamic mapping of the various Pages into the host addressable Upper Memory address space, whenever needed.

Note: The management memory map has been designed largely after the QSFP memory map. This memory map has been changed in order to accommodate 8 electrical lanes and to limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

8.1.2 Supported Pages

A basic 256 byte subset of the Management Memory Map is mandatory for all CMIS compliant devices. Other parts are only available for paged memory modules, or when advertised by the module. See Table 8-28 for details regarding the advertisement of supported management memory spaces.

In particular, support of the Lower Memory and of Page 00h is required for all modules, including passive copper cables. These pages are therefore always implemented. Additional support for Pages 01h, 02h and bank 0 of Pages 10h and 11h is required for all paged memory modules.

Bank 0 of pages 10h-1Fh, provides lane-specific registers for the first 8 lanes, and each additional bank provides support for additional 8 lanes. Note, however, that the allocation of information over the banks may be page specific and may not to be related to grouping data for 8 lanes.

The structure allows address space expansion for certain types of modules by allocating additional Pages. Moreover, additional banks of pages can be implemented to support modules with more than 8 lanes or for larger management memory needs.

[2] The actual storage structure of the memory pages is not in the scope of this specification. This specification only defines how the available memory pages can be addressed.

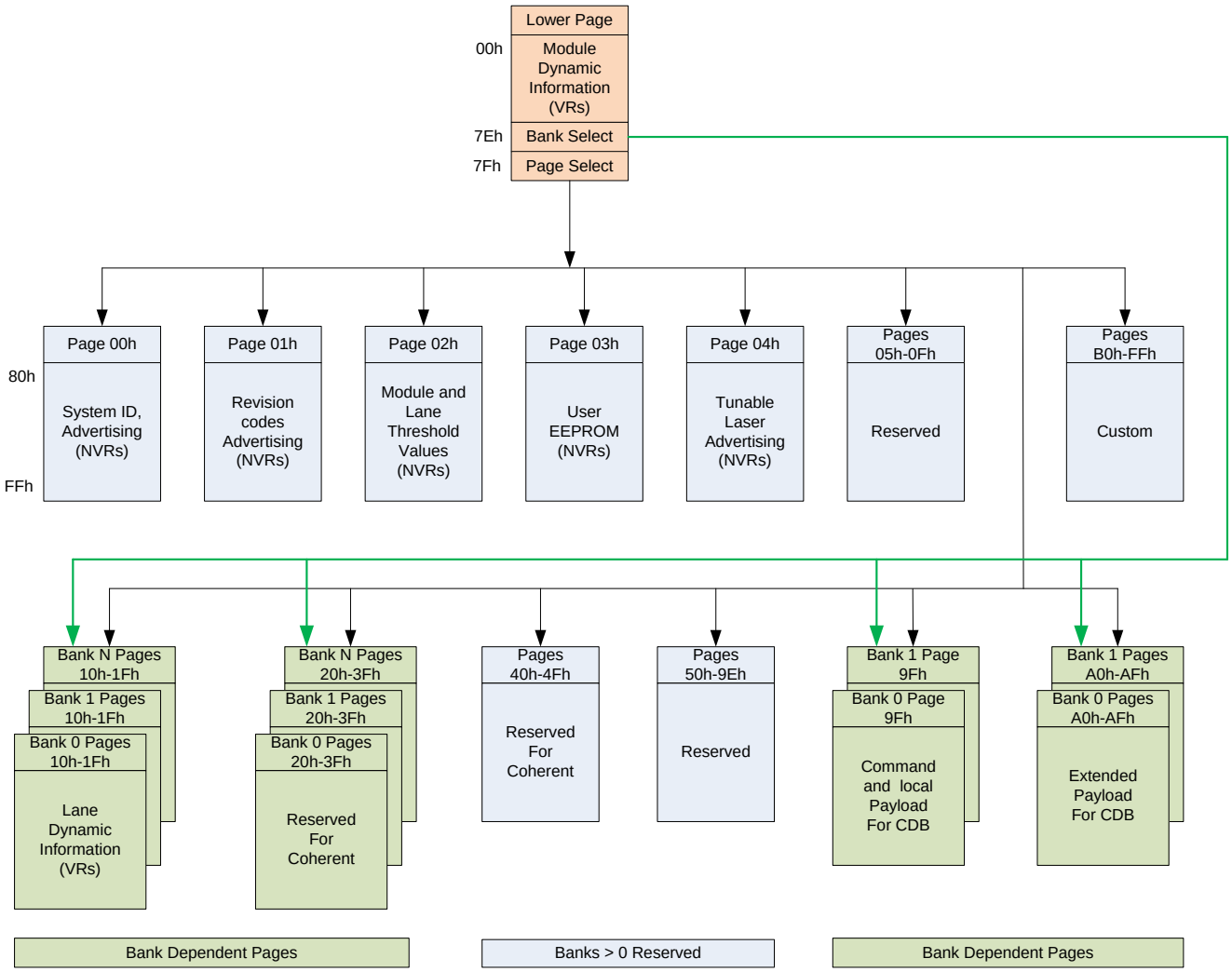


Figure 8-1 CMIS Module Memory Map

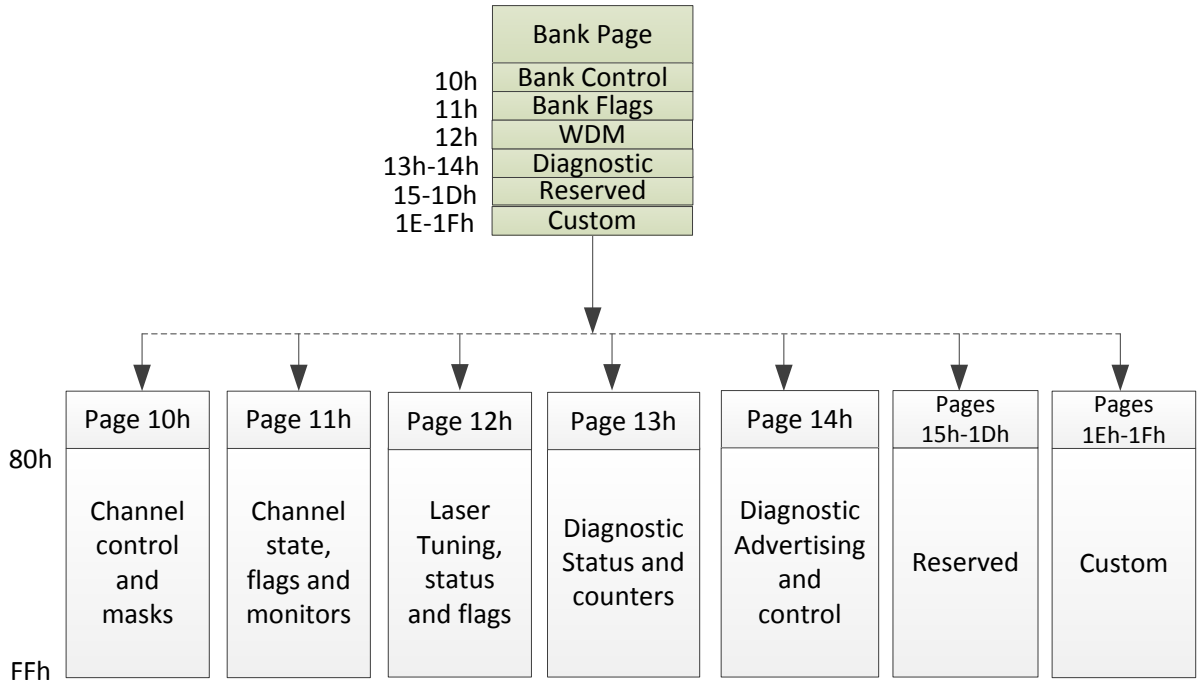


Figure 8-2 CMIS Bank Page Memory Map

8.1.3 General Specifications and Conventions

8.1.3.1 Referring to Bytes and Fields

Each byte in the internal management memory can be identified by an address triple consisting of a bank index (0-255), a page index (00h-FFh), and a byte address (0-255). The bank index 0 can be omitted for Pages without bank support. Bank index 0 and page number 00h can be omitted for the Lower Page.

With bits in a byte numbered from 0 to 7 per arithmetic significance, the following notation syntax may be used to identify each bit or bit field:

bank:page:byte.bit
bank:page:byte.bit-bit

8.1.3.2 Reserved Bytes, Fields, or Bits

Reserved locations (bytes, fields, or bits) are for future use and shall neither be used (evaluated) nor modified. The module shall zero-initialize reserved locations. There are no other obligations for the module. The results of forbidden host writes to reserved locations are undefined.

Other organizations shall contact the managing organization or the editor of this document to request allocations of register bytes, fields, or bits.

8.1.3.3 Custom Bytes or Fields

Custom bytes usage is not restricted and may be vendor defined. The use of registers defined as custom may be subject to additional agreements between module users and vendors.

8.1.3.4 Register Default Values

Default values for all control registers are 0 unless otherwise specified. Host implementers are encouraged to review critical registers and not rely on module default values. For Control Set registers the default settings may be Application dependent, see section 6.2.3.

8.2 Lower Memory Page 00h (Control and Status Essentials)

The Lower Memory consists of the lower 128 bytes of the 256 byte two-wire serial bus addressable space.

The Lower Page is used to access a variety of module level measurements, diagnostic functions and control functions, as well as to select which of the various Upper Pages in the structured memory map are accessed by byte addresses greater or equal than 128.

This portion of the 256 byte accessible address space is always directly addressable and thus is chosen for monitoring and control functions that may need to be repeatedly accessed.

The lower page is subdivided into several subject areas as shown in the following table:

Table 8-1 Lower Memory Overview

Address	Size	Subject Area	Description
0–3	4	ID and Status Area	Module ID from SFF-8024 list, version number, Type and status
			Flat mem indication, CLEI present indicator, Maximum TWI speed, Current state of Module, Current state of the Interrupt signal
4–7	4	Lane Flag Summary	Flag summary of all lane flags on pages 10h-1Fh
8-13	6	Module-Level Flags	All flags that are not lane or data path specific
14-25	12	Module-Level Monitors	Monitors that are not lane or data path specific
26-30	5	Module Global Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Flag Masks	Masking bits for the Module-Level flags
37-38	2	CDB Status Area	Status of most recent CDB command
39-40	2	Module Firmware Version	Module Firmware Version.
41-63	23	Reserved Area	Reserved for future standardization
64-82	19	Custom Area	Vendor or module type specific use
83-84	2	Inactive Firmware Version	Version Number of Inactive Firmware. Values of 00h indicates module supports only a single image.
85-117	33	Application Advertising	Combinations of host and media interfaces that are supported by module data path(s)
118-125	8	Password Entry and Change	
126	1	Bank Select Byte	Bank address of currently visible Page
127	1	Page Select Byte	Page address of currently visible Page

8.2.1 ID and Status

The ID and Status fields described in Table 8-2 provide fundamental memory map characteristics (module type, flat or paged memory, memory map version) as well as module status indicators.

Table 8-2 Identifier and Status Summary (Lower Page)

Byte	Bits	Field Name	Description	Type
0	7-0	Identifier	Identifier - Type of Serial Module - See SFF-8024.	RO RQD
1	7-0	Revision Compliance	Identifier – CMIS revision; the upper nibble is the whole number part and the lower nibble is the decimal part. Example: 01h indicates version 0.1, 21h indicates version 2.1.	RO RQD
2	7	Flat_mem	Upper memory flat or paged. 0b=Paged memory (pages 00h, 01h, 02h, 10h and 11h are implemented) 1b=Flat memory (only page 00h implemented)	RO RQD
	6	Reserved		
	5-4	Reserved		
	3-2	TWI Maximum speed	Indicates maximum two-wire serial speed supported by module 00b=Module supports up to 400 kHz 01b=Module supports up to 1 MHz 10b=Reserved 11b=Reserved	RO RQD
	1-0	Reserved		
3	7-4	Reserved		
	3-1	Module state	Current state of Module (see Table 8-3)	RO RQD
	0	Interrupt	Digital state of Interrupt output signal 0b=Interrupt asserted 1b=Interrupt not asserted (default)	

Table 8-3 Module State Encodings

Code	Module state
000b	Reserved
001b	ModuleLowPwr state
010b	ModulePwrUp state
011b	ModuleReady state (reported by flat memory modules)
100b	ModulePwrDn state
101b	Fault state
110b	Reserved
111b	Reserved

8.2.2 Lane Flag Summary

The lane flag summary bits identify which lane(s) flags are asserted in page 11h, for up to 4 banks of lanes. In order to clear the lane-specific flag, the lane flag itself must be read from page 11h on the appropriate bank.

Table 8-4 Lane Flag Summary (Lower Page)

Byte	Bit	Name	Description	Type
4	7	Bank 0 lane 8 flag summary	1b=one or more of the flag bits from bank 0, lane 8 is set.	RO RQD
	6	Bank 0 lane 7 flag summary	1b=one or more of the flag bits from bank 0, lane 7 is set.	RO RQD
	5	Bank 0 lane 6 flag summary	1b=one or more of the flag bits from bank 0, lane 6 is set.	RO RQD
	4	Bank 0 lane 5 flag summary	1b=one or more of the flag bits from bank 0, lane 5 is set.	RO RQD
	3	Bank 0 lane 4 flag summary	1b=one or more of the flag bits from bank 0, lane 4 is set.	RO RQD
	2	Bank 0 lane 3 flag summary	1b=one or more of the flag bits from bank 0, lane 3 is set.	RO RQD
	1	Bank 0 lane 2 flag summary	1b=one or more of the flag bits from bank 0, lane 2 is set.	RO RQD
	0	Bank 0 lane 1 flag summary	1b=one or more of the flag bits from bank 0, lane 1 is set.	RO RQD
5	7	Bank 1 lane 8 flag summary	1b=one or more of the flag bits from bank 1, lane 8 is set.	RO RQD
	6	Bank 1 lane 7 flag summary	1b=one or more of the flag bits from bank 1, lane 7 is set.	RO RQD
	5	Bank 1 lane 6 flag summary	1b=one or more of the flag bits from bank 1, lane 6 is set.	RO RQD
	4	Bank 1 lane 5 flag summary	1b=one or more of the flag bits from bank 1, lane 5 is set.	RO RQD
	3	Bank 1 lane 4 flag summary	1b=one or more of the flag bits from bank 1, lane 4 is set.	RO RQD
	2	Bank 1 lane 3 flag summary	1b=one or more of the flag bits from bank 1, lane 3 is set.	RO RQD
	1	Bank 1 lane 2 flag summary	1b=one or more of the flag bits from bank 1, lane 2 is set.	RO RQD
	0	Bank 1 lane 1 flag summary	1b=Indicates that one or more of the flag bits from bank 1, lane 1 is set.	RO RQD
6	7	Bank 2 lane 8 flag summary	1b=one or more of the flag bits from bank 2, lane 8 is set.	RO RQD
	6	Bank 2 lane 7 flag summary	1b=one or more of the flag bits from bank 2, lane 7 is set.	RO RQD
	5	Bank 2 lane 6 flag summary	1b=one or more of the flag bits from bank 2, lane 6 is set.	RO RQD
	4	Bank 2 lane 5 flag summary	1b=one or more of the flag bits from bank 2, lane 5 is set.	RO RQD
	3	Bank 2 lane 4 flag summary	1b=Indicates that one or more of the flag bits from bank 2, lane 4 is set.	RO RQD
	2	Bank 2 lane 3 flag summary	1b=Indicates that one or more of the flag bits from bank 2, lane 3 is set.	RO RQD
	1	Bank 2 lane 2 flag summary	1b=Indicates that one or more of the flag bits from bank 2, lane 2 is set.	RO RQD
	0	Bank 2 lane 1 flag summary	1b=Indicates that one or more of the flag bits from bank 2, lane 1 is set.	RO RQD
7	7	Bank 3 lane 8 flag summary	1b=one or more of the flag bits from bank 3, lane 8 is set.	RO RQD
	6	Bank 3 lane 7 flag summary	1b=one or more of the flag bits from bank 3, lane 7 is set.	RO RQD
	5	Bank 3 lane 6 flag summary	1b=one or more of the flag bits from bank 3, lane 6 is set.	RO RQD
	4	Bank 3 lane 5 flag summary	1b=one or more of the flag bits from bank 3, lane 5 is set.	RO RQD
	3	Bank 3 lane 4 flag summary	1b=one or more of the flag bits from bank 3, lane 4 is set.	RO RQD
	2	Bank 3 lane 3 flag summary	1b=one or more of the flag bits from bank 3, lane 3 is set.	RO RQD
	1	Bank 3 lane 2 flag summary	1b=one or more of the flag bits from bank 3, lane 2 is set.	RO RQD
	0	Bank 3 lane 1 flag summary	1b=one or more of the flag bits from bank 3, lane 1 is set.	RO RQD

8.2.3 Module-Level Flags

This section of the memory map contains module-level flags. These flags provide a mechanism for reporting module-level status changes, faults, operating failures and alarms and warnings for monitored attributes. Each module-level flag shall have an associated flag mask. Monitored attributes with associated alarm and/or warning thresholds shall implemented associated alarm and warning flags and flag masks. For normal operation and default state, the bits in this field have the value of 0b. Once asserted, the bits remain set (latched) until cleared by a read operation that includes the affected bit or reset by the Reset signal. Note that a read of the flag summary shall not clear the underlying flag condition. If the corresponding mask bit is not set (see Table 8-8), Interrupt is also asserted at the onset of the condition and remains asserted until all asserted flags (both module-level and lane-specific) have been cleared by a host read. After being read and cleared, the bit shall be set again if the condition persists; this will cause Interrupt to be asserted again unless masked. The module-level flags are defined in Table 8-5. Byte 13 is provided for Custom Module Level Flags. Some module-level flags are disallowed in certain Module States, refer to section 6.3.3 for details.

Table 8-5 Module Flags (Lower Page, active modules only)

Byte	Bit	Name	Description	Type
8	7	L-CDB block 2 complete	Latched flag to indicate completion of the CDB command for CDB block 2. Clear on Read (See Page 01h, Byte 163 bit 7)	RO Opt.
	6	L-CDB block 1 complete	Latched flag to indicate completion of the CDB command for CDB block 1. Clear on Read (See Page 01h, Byte 163 bit 6)	RO Opt.
	5-3	Reserved		RQD
	2	Data Path firmware fault	Some modules may contain an auxiliary device for processing the transmitted and received signals (e.g. a DSP). The Data Path Firmware Fault flag becomes set when an integrity check of the firmware for this auxiliary device finds an error.	RO Opt.
	1	Module firmware fault	The Module Firmware Fault flag becomes set when an integrity check of the module firmware finds an error. There are several possible causes of the error such as program memory becoming corrupted and incomplete firmware loading.	RO Opt.
	0	L-Module state changed flag	Latched Indication of change of Module state (see Table 8-5) Clear on Read	RO RQD
9	7	L-Vcc3.3v Low Warning	Latched low 3.3 volts supply voltage warning flag. Clear on Read	RO Opt.
	6	L-Vcc3.3v High Warning	Latched high 3.3 volts supply voltage warning flag. Clear on Read	
	5	L-Vcc3.3v Low Alarm	Latched low 3.3 volts supply voltage alarm flag. Clear on Read	
	4	L-Vcc3.3v High Alarm	Latched high 3.3 volts supply voltage alarm flag. Clear on Read	
	3	L-Temp Low Warning	Latched low temperature warning flag. Clear on Read	
	2	L-Temp High Warning	Latched high temperature warning flag. Clear on Read	
	1	L-Temp Low Alarm	Latched low temperature alarm flag. Clear on Read	
	0	L-Temp High Alarm	Latched high temperature alarm flag. Clear on Read	
10	7	L-Aux 2 Low Warning	Latched low warning for Aux 2 monitor. Clear on Read	RO Opt.
	6	L-Aux 2 High Warning	Latched high warning for Aux 2 monitor. Clear on Read	
	5	L-Aux 2 Low Alarm	Latched low alarm for Aux 2 monitor. Clear on Read	
	4	L-Aux 2 High Alarm	Latched high alarm for Aux 2 monitor. Clear on Read	
	3	L-Aux 1 Low Warning	Latched low warning for Aux 1 monitor. Clear on Read	
	2	L-Aux 1 High Warning	Latched high warning for Aux 1 monitor. Clear on Read	
	1	L-Aux 1 Low Alarm	Latched low alarm for Aux 1 monitor. Clear on Read	
	0	L-Aux 1 High Alarm	Latched high alarm for Aux 1 monitor. Clear on Read	

Byte	Bit	Name	Description	Type
11	7	L-Vendor Defined Low Warning	Latched low warning for Vendor Defined Monitor. Clear on Read	RO Opt.
	6	L-Vendor Defined High Warning	Latched high warning for Vendor Defined Monitor. Clear on Read	
	5	L-Vendor Defined Low Alarm	Latched low alarm for Vendor Defined Monitor. Clear on Read	
	4	L-Vendor Defined High Alarm	Latched high alarm for Vendor Defined Monitor. Clear on Read	
	3	L-Aux 3 Low Warning	Latched low warning for Aux 3 monitor. Clear on Read	
	2	L-Aux 3 High Warning	Latched high warning for Aux 3 monitor. Clear on Read	
	1	L-Aux 3 Low Alarm	Latched low alarm for Aux 3 monitor. Clear on Read	
	0	L-Aux 3 High Alarm	Latched high alarm for Aux 3 monitor. Clear on Read	
12	7-0	Reserved		
13	7-0	Custom		

8.2.4 Module-Level Monitors

Real time monitoring for the module includes temperature, supply voltage, auxiliary and vendor defined monitors as shown in Table 8-6.

The data format may facilitate greater resolution and range than required. Measurement accuracy is defined by the interoperability standard or module product specification.

Table 8-6 Module Monitors (Lower Page, active modules only)

Byte	Bit	Name	Description	Type
14	7-0	Module Monitor 1: Temperature MSB	Internally measured temperature: signed 2's complement in 1/256 degree Celsius increments NOTE: Temp can be below 0.	RO Opt.
15	7-0	Module Monitor 1: Temperature1 LSB		
16	7-0	Module Monitor 2: Supply 3.3-volt MSB	Internally measured 3.3 volt input supply voltage: in 100 µV increments	RO Opt.
17	7-0	Module Monitor 2: Supply 3.3-volt LSB		
18	7-0	Module Monitor 3: Aux 1 MSB	TEC Current or Reserved monitor TEC Current: signed 2's complement in 1/32767% increments of maximum TEC current +32767 is max TEC current (100%) – Max Heating -32767 is min TEC current (100%) – Max Cooling	RO Opt.
19	7-0	Module Monitor 3: Aux 1 LSB		
20	7-0	Module Monitor 4: Aux 2 MSB	TEC Current or Laser Temperature monitor TEC Current: signed 2's complement in 1/32767% increments of maximum TEC current +32767 is max TEC current (100%) – Max Heating -32767 is min TEC current (100%) – Max Cooling Laser Temperature: signed 2's complement in 1/256 degree Celsius increments See Page 01h Byte 145 Table Table 8-30	RO Opt.
21	7-0	Module Monitor 4: Aux 2 LSB		
22	7-0	Module Monitor 5: Aux 3 MSB	Laser Temperature or additional supply voltage monitor Laser Temperature: signed 2's complement in 1/256 degree Celsius increments Additional supply voltage monitor: in 100 µV increments See Page 01h Byte 145 Table Table 8-30	RO Opt.
23	7-0	Module Monitor 5: Aux 3 LSB		

Byte	Bit	Name	Description	Type
24	7-0	Module Monitor 6: Custom MSB	Custom monitor	RO Opt.
25	7-0	Module Monitor 6: Custom LSB		

8.2.5 Module Global Controls

Module global controls are control aspects that are applicable to the entire module or all channels in the module.

Note: Lane-specific controls are located in Upper page 10h (section 8.7.2).

Table 8-7 Module Global and Squelch Mode Controls (Lower Page, active modules only)

Byte	Bit	Name	Description	Type
26	7	Reserved		
	6	LowPwr	A parameter used to control the module power mode. See section 6.3.1.1 for usage Default value = 1	RW RQD
	5	Squelch control	0b=Tx Squelch reduces OMA 1b=Tx Squelch reduces Pave (See Table 8-31 for capability advertising)	RW Opt.
	4	ForceLowPwr	1b=Forces module into low power mode – see section 6.3.1.3	RW RQD
	3	Software Reset	Self-clearing bit that causes the module to be reset. The effect is the same as asserting the ResetL signal for the appropriate hold time, followed by its de-assertion. This bit will be cleared to zero on a reset so a value of 0 will always be returned. 0b=Not in reset 1b=Software reset	RW RQD
	2-0	Custom		
27-28	All	Reserved		
29-30	All	Custom	Custom Global controls	

8.2.6 Module-Level Flag Masks

The host may control which flags may cause a hardware Interrupt being asserted to the host by setting masking bits in Table 8-8.

For each flag bit there is a corresponding masking bit. Masking bits are set when their value is or becomes 1. Masking bits are cleared when their value is or becomes 0.

The module behaves as follows: a set masking bit prevents assertion of the hardware interrupt signal by the corresponding latched flag bit. A cleared masking bit, when the corresponding flag bit is the only reason for the hardware Interrupt signal being asserted, de-asserts the hardware Interrupt signal. Masking bits are volatile: at exit from MgmtInit (see section 6.3.1.6), all mask bits shall be clear.

The host may use the masking bits to prevent continued hardware Interrupt assertion from stable conditions, i.e. from asserted flag bits, which would otherwise continually reassert the hardware Interrupt signal.

Table 8-8 Module Level Flag Masks (Lower Page, active modules only)

Byte	Bits	Name	Description	Type
31	7	M-CDB Block 2	Masking bit for CDB Block 2 Complete flag	RW

Byte	Bits	Name	Description	Type
		complete		Opt.
	6	M-CDB Block 1 complete	Masking bit for CDB Block 1 Complete flag	RW Opt.
	5-3	Reserved		RO
	2	M-Data Path firmware fault	Masking bit for Data Path Firmware Fault flag	RW Opt.
	1	M-Module firmware fault	Masking bit for Module Firmware Fault flag	RW Opt.
	0	M-Module State changed flag mask	Masking bit for Module State Changed flag	RW RQD
32	7	M-Vcc3.3 Low Warning flag mask	Masking bit for Vcc3.3 monitor low warning flag	RW Opt.
	6	M-Vcc3.3 High Warning flag mask	Masking bit for Vcc3.3 monitor high warning flag	
	5	M-Vcc3.3 Low Alarm flag mask	Masking bit for Vcc3.3 monitor low alarm flag	
	4	M-Vcc3.3 High Alarm flag mask	Masking bit for Vcc3.3 monitor high alarm flag	
	3	M-Temp Low Warning flag mask	Masking bit for temperature monitor low warning flag	
	2	M-Temp High Warning flag mask	Masking bit for temperature monitor high warning flag	
	1	M-Temp Low Alarm flag mask	Masking bit for temperature monitor low alarm flag	
	0	M-Temp High Alarm flag mask	Masking bit for temperature monitor high alarm flag	
33	7	M-Aux 2 Low Warning flag mask	Masking bit for Aux 2 monitor low warning flag	RW Opt.
	6	M-Aux 2 High Warning flag mask	Masking bit for Aux 2 monitor high warning flag	
	5	M-Aux 2 Low Alarm flag mask	Masking bit for Aux 2 monitor low alarm flag	
	4	M-Aux 2 High Alarm flag mask	Masking bit for Aux 2 monitor high alarm flag	
	3	M-Aux 1 Low Warning flag mask	Masking bit for Aux 1 monitor low warning flag	
	2	M-Aux 1 High Warning flag mask	Masking bit for Aux 1 monitor high warning flag	
	1	M-Aux 1 Low Alarm flag mask	Masking bit for Aux 1 monitor low alarm flag	
	0	M-Aux 1 High Alarm flag mask	Masking bit for Aux 1 monitor high alarm flag	
34	7	M-Vendor Defined Low Warning flag mask	Masking bit for Vendor defined low warning flag	RW Opt.
	6	M-Vendor Defined High Warning flag mask	Masking bit for Vendor defined high warning flag	
	5	M-Vendor Defined Low Alarm flag mask	Masking bit for Vendor defined low alarm flag	
	4	M-Vendor Defined High Alarm flag mask	Masking bit for Vendor defined high alarm flag	
	3	M-Aux 3 Low Warning flag mask	Masking bit for Aux 3 monitor low warning flag	
	2	M-Aux 3 High Warning	Masking bit for Aux 3 monitor high warning flag	

Byte	Bits	Name	Description	Type
		flag mask		
	1	M-Aux 3 Low Alarm flag mask	Masking bit for Aux 3 monitor low alarm flag	
	0	M-Aux 3 High Alarm flag mask	Masking bit for Aux 3 monitor high alarm flag	
35	7-0	Reserved flag mask		
36	7-0	Custom	Module level flag masks	

8.2.7 CDB Status

The CDB Status fields provide the status of the most recently triggered CDB command. For modules that support CDB background operation (see Table 8-35), the host may read the CDB Status field while a CDB command is executing to obtain its current status. For modules that do not support CDB background operation, the host may read the CDB status field after the command has completed, determined through NACK polling.

Table 8-9 CDB Status fields (Lower Page, active modules only)

Byte	Bits	Name	Description	Type
37	7-0	CDB Block 1 status	Status of the most recently triggered CDB command in CDB Block 1	RO Opt.
38	7-0	CDB Block 2 status	Status of the most recently triggered CDB command in CDB Block 2	RO Opt.

Each CDB Status field has the following format:

Table 8-10 Bit definitions within CDB Status fields (Lower Page, active modules only)

Bits	Name	Description
7	STS_BUSY	One-bit value indicating the availability of the CDB interface 0b=Module idle, host can write 1b=Module busy, host needs to wait
6	STS_FAIL	0b=Last triggered CDB command completed successfully 1b=Last triggered CDB command failed, see Last Command Result field for details
5-0	Last command result	**Note: The following fields depend on the values of bits 6,7.** **STS_BUSY=1, STS_FAIL=X (IN PROGRESS)** 00h=Reserved 01h=Command is captured but not processed 02h=Command checking is in progress 03h=Command execution is in progress 04h-2Fh=Reserved 30h-3Fh=Custom **STS BUSY=0, STS_FAIL=0 (SUCCESS)** 00h=Reserved 01h=Command completed successfully without specific message 02h=Reserved 03h=Previous CMD was ABORTED by CMD Abort 04h-1Fh=Reserved 20h-2Fh=Reserved 30h-3Fh=Custom **STS_BUSY=0, STS_FAIL=1 (FAILED)** 00h=Reserved 01h=CMD Code unknown 02h=Parameter range error or not supported

Bits	Name	Description
		03h=Previous CMD was not ABORTED by CMD Abort 04h=Command checking time out 05h=CdbCheckCode Error 06h=Password error 07h-0Fh=Reserved for STS command checking error 10h-1Fh=Reserved 20h-2Fh=For individual STS command or task error 30h-3Fh=Custom

Each CDB status field is located in lower memory so that page changes are not needed to read it. Both of these fields are initialized to 0 before exiting MgmtInit (see section 6.3.1.6).

The module updates the STS_BUSY bit to 1b when a CDB command is triggered on the respective block. When a CDB command completes, the module sets the STS_BUSY bit to 0b and sets the STS_FAIL and Last Command Result fields according to the result of the completed command. All subfields within a CDB Status byte remain unchanged until the next CDB command is triggered for the respective block.

8.2.8 Module Active Firmware Version

Bytes in Table 8-9 allows a module to return the active (current running) firmware major and minor revision. Flat memory modules that has firmware running may report it's firmware version in these bytes.

The encoding or major and minor revision are:

- Major Revision = 0 and Minor Revision = 0 indicates that a module does not have any firmware.
- Major Revision = FFh and Minor Revision = FFh indicates that a module active firmware image is bad.
- All other Major and Minor Revision combinations are used to indicate the active firmware version.

Table 8-11 Module Active Firmware Version

Byte	Bits	Name	Description	Type
39	7-0	Active Module firmware major revision	Numeric representation of Active module firmware major revision	RO Opt.
40	7-0	Active Module firmware minor revision	Numeric representation of Active module firmware minor revision	RO Opt.

A module having an active firmware version may or may not have an inactive version. A module supporting paged memory may also advertise an inactive image in the bytes described in section 8.4.1 which has the same encodings. Content of the firmware major and minor revisions reported back are vendor dependent. Modules that supports a proprietary vendor dependent firmware upgrade methodology (not CDB as described later) may still report firmware active or inactive versions in these bytes.

8.2.9 Application Advertising

Table 8-13 provides space for the first four bytes of up to eight Application descriptors. The remaining fifth byte (Media Lane Assignment Options) of each Application descriptor is stored in a separate Table 8-38.

All modules shall advertise at least one Application. The Host Electrical Interface ID field of the first unused entry in Table 8-13 shall be set to a value of FFh to indicate the end of the list of valid Application descriptors.

When more than eight Applications need to be advertised, additional Application descriptors can be stored in Table 8-39 and in the second half of Table 8-38.

Note: Application descriptors are used by the module to advertise supported Applications. See section 6.2.1.1 for more information about Application advertising .

Host Electrical Interface IDs and Module Media Interface IDs are specified in SFF-8024.

The Module Type Encoding field (Byte 85) indicates which particular Media Interface Type table applies to the module. Valid Module Type Encoding values are specified in Table 8-12.

The host lane count and media lane count fields specify the number of lanes either explicitly (nonzero value) or by implicit reference, via the interface ID, to the relevant interface specification (zero value).

The host lane assignment options specify which lane groups can be used for a Data Path carrying the advertised application. Bits 0-7 form a bit map corresponding to Host Lanes 1-8. A bit value of 1 indicates that the lane group of the advertised Application can begin on the corresponding host lane. See section 6.2.1.1 for a more detailed description.

Table 8-12 Byte 85 Module Media Type Encodings (Type RO RQD)

Code	Module Media Type	Associated Interface ID Table
00h	Undefined	
01h	Optical Interfaces: MMF	SFF-8024 IDs for 850 nm Multi-Mode Media Interfaces
02h	Optical Interfaces: SMF	SFF-8024 IDs for 1300/1550 nm Single Mode Media Interfaces
03h	Passive Cu	SFF-8024 IDs for Passive Copper Cable Media Interfaces
04h	Active Cables	SFF-8024 IDs for Active Cable Assembly Media Interfaces
05h	BASE-T	SFF-8024 IDs for Base-T Media Interfaces
06h-3Fh	Reserved	
40h-8Fh	Custom	
90h-FFh	Reserved	

Table 8-13 Application Advertising Fields (Lower page)

Byte	Bits	ApSel Code	Name	Description	Type
86	7-0		Host Electrical Interface ID	ID from SFF-8024 IDs for Host Electrical Interfaces	RO RQD
87	7-0		Module Media Interface ID	ID from table selected by Byte 85 (see Table 8-12)	
88	7-4		Host Lane Count	0000b=lane count defined by interface ID 0001b=1 lane, 0010b=2 lanes .... 1000b=8 lanes. 1001b-1111b=reserved	
	3-0	0001b	Media Lane Count		
89	7-0		Host Lane Assignment Options (See Table 8-38 for Media Lane Assignment Options)	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit value 1 indicates that the Application may begin on the corresponding host lane. Refer to section 6.2.1.1 for details.	
90	7-0		Host Electrical Interface ID	See ApSel Code 0001b Coded FFh if first unused ApSel code	RO Opt.
91	7-0	0010b	Module Media Interface ID	See ApSel Code 0001b	
92	7-4		Host Lane Count	See ApSel Code 0001b	
	3-0		Media Lane Count		
93	7-0		Host Lane Assign Options	See ApSel Code 0001b	
94	7-0		Host Electrical Interface ID	See ApSel Code 0001b	RO Opt.
95	7-0		Module Media Interface ID	See ApSel Code 0001b	
96	7-4	0011b	Host Lane Count	See ApSel Code 0001b	
	3-0		Media Lane Count		
97	7-0		Host Lane Assign Options	See ApSel Code 0001b	
98	7-0		Host Electrical Interface ID	See ApSel Code 0001b	RO Opt.
99	7-0		Module Media Interface ID	See ApSel Code 0001b	
100	7-4	0100b	Host Lane Count	See ApSel Code 0001b	
	3-0		Media Lane Count		
101	7-0		Host Lane Assign Options	See ApSel Code 0001b	
102	7-0		Host Electrical Interface ID	See ApSel Code 0001b	RO Opt.
103	7-0		Module Media Interface ID	See ApSel Code 0001b	
104	7-4	0101b	Host Lane Count	See ApSel Code 0001b	
	3-0		Media Lane Count		
105	7-0		Host Lane Assign Options	See ApSel Code 0001b	
106	7-0		Host Electrical Interface ID	See ApSel Code 0001b	RO Opt.
107	7-0		Module Media Interface ID	See ApSel Code 0001b	
108	7-4	0110b	Host Lane Count	See ApSel Code 0001b	
	3-0		Media Lane Count		
109	7-0		Host Lane Assign Options	See ApSel Code 0001b	
110	7-0		Host Electrical Interface ID	See ApSel Code 0001b	RO Opt.
111	7-0		Module Media Interface ID	See ApSel Code 0001b	
112	7-4	0111b	Host Lane Count	See ApSel Code 0001b	
	3-0		Media Lane Count		
113	7-0		Host Lane Assign Options	See ApSel Code 0001b	
114	7-0		Host Electrical Interface ID	See ApSel Code 0001b	RO Opt.
115	7-0		Module Media Interface ID	See ApSel Code 0001b	
116	7-4	1000b	Host Lane Count	See ApSel Code 0001b	
	3-0		Media Lane Count		
117	7-0		Host Lane Assign Options	See ApSel Code 0001b	

8.2.10 Password Entry and Change

The host system manufacturer password shall fall in the range of 00000000h to 7FFFFFFFh, and all module manufacturer passwords in the range of 80000000h to FFFFFFFFh. The host system manufacturer password shall be initially set to 00001011h in new modules.

The host system manufacturer password may be changed by writing a new password in Bytes 118-121 when the correct current host system manufacturer password has been entered in Bytes 122-125, with the high order bit being ignored and forced to a value of 0 in the new password. The password entry field shall be set to 00000000h on power up and reset.

Table 8-14 Password Change Entry

Byte	Bits	Name	Description	Type
118-121	7-0	Password Change Entry Area		WO Opt.
122-125	7-0	Password Entry Area		WO Opt.

8.2.11 Bank Select Byte

The value written to the Bank Select byte 126 determines which bank is accessed when banking is supported.

The host shall write the bank select and page select registers in one TWI transaction when a bank change is required, even if the page number is not changing.

The module shall not begin processing the new bank select setting until after the page select register is written.

Writing the value of a non-supported bank shall be ignored by the module. The Bank Select byte shall also be ignored if the memory map address being accessed is less than or equal to 127.

Writing the value of a non-supported bank and page combination shall not be accepted by the module. In this case the module shall set the Page Select byte to 0. Since page 00h is less than 10h, the module ignores the invalid bank select byte and returns the contents of page 00h in subsequent memory map read/write operations.

8.2.12 Page Select Byte

The value of the Page Select byte 127 determines which page is accessed when a TWI based read or write command accesses byte addresses 128 through 255.

A value of 00h indicates Page 00h is mapped to Bytes 128-255 and a value of 01h indicates that Page 01h if available is mapped to Bytes 128-255. Similarly, values of 02h, 03h, etc., indicate that the page identified by the bank select byte is mapped to Bytes 128-255.

Writing the value of a non-supported page or a non-supported bank and page combination shall not be accepted by the module. In such cases the Page Select byte shall revert to 0 and read/write operations shall be to page 00h.

For a bank change, the host shall write the Bank Select and Page Select registers in the same TWI transaction.

8.3 Upper Memory - Page 00h (Administrative Information)

Upper page 00h contains static read-only module identification information. Upper page 00h shall be implemented for both paged and flat memory implementations and is required for all modules and cable assemblies.

Table 8-15 Page 00h Overview

Address	Size (bytes)	Name	Description
128	1	Identifier	Identifier Type of module
129-144	16	Vendor name	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	Date Code	
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power characteristics	
202	1	Cable assembly length	
203	1	Media Connector Type	
204-209	6	Copper Cable Attenuation	
210-211	2	Cable Assembly Lane Information	
212	1	Media Interface Technology	
213-220	8	Reserved	
221	1	Custom	
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	

8.3.1 Identifier

The identifier value specifies the physical device implementation and, by inference, memory map data format. This field should contain the same value as byte 0 in lower memory. These values are maintained in the Transceiver Management section of SFF-8024.

Table 8-16 Identifiers (Page 00h)

Byte	Bits	Name	Description	Type
128	7-0	Identifier	Identifier - Type of Serial Module - See SFF-8024.	RO RQD

8.3.2 Vendor Name (Page 00h, Bytes 129-144, RO, required)

The vendor name is a required 16 character field (bytes 129-144) that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name of the corporation, the SCSI company code for the corporation, or the stock exchange code for the corporation. The vendor name may be the original manufacturer of the module or the name of the module reseller. In both cases, the Vendor Name and Vendor OUI (if specified) shall correlate to the same company. At least one of the vendor name or the vendor OUI fields shall contain valid serial data.

8.3.3 Vendor Organizationally Unique Identifier (Page 00h, Bytes 145-147, RO, required)

The vendor organizationally unique identifier field (vendor OUI) is a required 3-byte field (bytes 145-147) that contains the IEEE Company Identifier for the vendor. A value of all zero in the 3-byte field indicates that the Vendor OUI is unspecified.

8.3.4 Vendor Part Number (Page 00h, Bytes 148-163, RO, required)

The vendor part number (vendor PN) is a required 16-byte field (bytes 148-163) that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor part number or product name. A value of all zero in the 16-byte field indicates that the vendor part number is unspecified.

8.3.5 Vendor Revision Number (Page 00h, Bytes 164-165, RO, required)

The vendor revision number (vendor rev) is a required 2-byte field (bytes 164-165) that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor's product revision number. A value of all zero in the field indicates that the vendor Rev is unspecified.

8.3.6 Vendor Serial Number (Page 00h, Bytes 166-181, RO, required)

The vendor serial number (vendor SN) is a required 16-character field (bytes 166-181) that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor's serial number for the Product. A value of all zero in the 16-byte field indicates that the vendor serial number is unspecified.

8.3.7 Date Code

The date code is an 8-byte field that contains the vendor's date code in ASCII characters. The date code is mandatory. The date code shall be in the following format:

Table 8-17 Date Code (Page 00h)

Byte	Bits	Name	Description	Type
182-183	All	Date code year	ASCII code, two low order digits of year (00=2000)	RO RQD
184-185	All	Date code month	ASCII code digits of month (01=Jan through 12=Dec)	RO RQD
186-187	All	Date code day of month	ASCII code day of month (01-31)	RO RQD
188-189	All	Lot code	ASCII code, custom lot code, may be blank	RO Opt.

8.3.8 CLEI Code

The CLEI (Common Language Equipment Identification) code is a 10-byte field (bytes 190-199) that contains the vendor's CLEI code in ASCII characters. The CLEI code is optional. If CLEI code is not implemented a value of ASCII 20h (space) shall be entered.

8.3.9 Module Power Characteristics

The module power characteristics are defined in the two memory locations in Table 8-18. The power class identifier and max power field both specify maximum power consumption over operating conditions and lifetime with all supported settings set to worst case values. See section 6.3.1.3 for details.

Table 8-18 Module Power Class and Max Power (Page 00h)

Byte	Bits	Name	Description	Type
200	7-5	Module Card Power Class[1]	000: Power class 1 001: Power class 2 010: Power class 3 011: Power class 4 100: Power class 5 101: Power class 6 110: Power class 7 111: Power class 8 (see byte 201)	RO RQD
	4-0	Reserved		RO
201	7-0	Max Power	Maximum power consumption in multiples of 0.25 W rounded up to the next whole multiple of 0.25 W	RO RQD

Note 1: See hardware specification for Power class values

8.3.10 Cable Assembly Length

The link length field provides the physical interconnect length of cable assemblies, including both passive copper and active optical or electrical cables. Transceivers with separable optical connectors shall populate this field with a 0. The code 11111111b means that the device supports a link length greater than 6300 m.

Table 8-19 Cable Assembly Length (Page 00h)

Byte	Bits	Name	Description	Type
202	7-6	Length multiplier field (Copper or active cable)	Multiplier for value in bits 5-0. 00 = multiplier of 0.1 01 = multiplier of 1 10 = multiplier of 10 11 = multiplier of 100	RO RQD
	5-0	Base Length field (copper of active cable)	Link length base value in meters. To calculate actual link length use multiplier in bits 7-6.	

8.3.11 Media Connector Type

The Connector Type field indicates the connector type for the media side of the module. These values are maintained in the Connector References section of SFF-8024.

Table 8-20- Media Connector Type (Page 00h)

Byte	Bits	Name	Description	Type
203	7-0	Connector Type	Type of connector present in the module. See SFF-8024 for codes.	RO RQD

8.3.12 Copper Cable Attenuation

These Bytes are used to define the cable attenuation for passive copper cables. For transceiver modules bytes 204-209 are reserved.

Table 8-21 Copper Cable Attenuation (Page 00h)

Byte	Bits	Name	Description	Type
204	7-0	5 GHz attenuation	Passive copper cable attenuation at 5 GHz in 1 dB increments	RO Opt.
205	7-0	7 GHz attenuation	Passive copper cable attenuation at 7 GHz in 1 dB increments	RO Opt.
206	7-0	12.9 GHz attenuation	Passive copper cable attenuation at 12.9 GHz in 1 dB increments	RO Opt.
207	7-0	25.8 GHz attenuation	Passive copper cable attenuation at 25.8 GHz in 1 dB increments	RO Opt.
208-209	All	reserved		RO

8.3.13 Cable Assembly Lane Information

Table 8-22 (Byte 210) is applied to all modules to indicate the number of near end media lanes implemented. With optical cable assemblies a media lane may be a fiber or a wavelength. Far end cable lane group fields (Byte 211) are used for cable assemblies to indicate the number of far end lanes implemented and the far end lane configuration. Far end cable lane group fields do not apply to modules with detachable media connectors. No information is given on the type of module on the far end of the cable (i.e. QSFP, SFP etc.), only the number of modules in the far end.

Table 8-22- Media lane interface implementation (Page 00h)

Byte	Bits	Name	Description	Type
210	7	Near end implementation lane 8	0b=Lane 8 implemented in near end 1b=Lane 8 not implemented in near end	RO Opt.
	6	Near end implementation lane 7	0b=Lane 7 implemented in near end 1b=Lane 7 not implemented in near end	
	5	Near end implementation lane 6	0b=Lane 6 implemented in near end 1b=Lane 6 not implemented in near end	
	4	Near end implementation lane 5	0b=Lane 5 implemented in near end 1b=Lane 5 not implemented in near end	
	3	Near end implementation lane 4	0b=Lane 4 implemented in near end 1b=Lane 4 not implemented in near end	
	2	Near end implementation lane 3	0b=Lane 3 implemented in near end 1b=Lane 3 not implemented in near end	
	1	Near end implementation lane 2	0b=Lane 2 implemented in near end 1b=Lane 2 not implemented in near end	
	0	Near end implementation lane 1	0b=Lane 1 implemented in near end 1b=Lane 1 not implemented in near end	
211	7-5	Reserved		RO
	4-0	Far End Configuration	See Table 8-23 for config code of discrete far end connectors	RO Opt.

Table 8-23 contains codes for all near end supported combinations of far end modules (lane groups a to h), and maps those far end modules (lane groups) to the connected near end lane number. Unique letters indicate discrete modules. Note that the discrete modules may or may not be the same module type.

Table 8-23 Far end cable lane groups advertising codes (Page 00h)

Far End Cable Lane Groups Advertising Codes									
Config Code		Near End Host Lane Number							
Decimal	Binary	1	2	3	4	5	6	7	8
0	00000b	Undefined - Use for detachable modules							
1	00001b	a	b	c	d	e	f	g	h
2	00010b	a	a	a	a	a	a	a	a
3	00011b	a	a	a	a	e	e	e	e
4	00100b	a	b	c	d	e	e	e	e
5	00101b	a	b	c	c	e	e	e	e
6	00110b	a	a	c	d	e	e	e	e
7	00111b	a	a	c	c	e	e	e	e
8	01000b	a	a	a	a	e	f	g	h
9	01001b	a	a	a	a	e	f	g	g
10	01010b	a	a	a	a	e	e	g	h
11	01011b	a	a	a	a	e	e	g	g
12	01100b	a	a	c	c	e	e	g	g
13	01101b	a	b	c	c	e	e	g	g
14	01110b	a	a	c	d	e	e	g	g
15	01111b	a	b	c	d	e	e	g	g
16	10000b	a	a	c	c	e	f	g	g
17	10001b	a	b	c	c	e	f	g	g
18	10010b	a	a	c	d	e	f	g	g
19	10011b	a	b	c	d	e	f	g	g
20	10100b	a	a	c	c	e	e	g	h
21	10101b	a	b	c	c	e	e	g	h
22	10110b	a	a	c	d	e	e	g	h
23	10111b	a	b	c	d	e	e	g	h
24	11000b	a	a	c	c	e	f	g	h
25	11001b	a	b	c	c	e	f	g	h
26	11010b	a	a	c	d	e	f	g	h
27-31	11011b-11111b	reserved							

8.3.14 Media Interface Technology (required)

Byte 212 is a required byte that defines aspects of the device or cable technology, using the encodings in Table 8-24. An active optical cable may distinguish from a separable module using Byte 203 (see section 8.3.11).

Table 8-24 Media Interface Technology encodings

Code	Description of physical device
00h	850 nm VCSEL
01h	1310 nm VCSEL
02h	1550 nm VCSEL
03h	1310 nm FP
04h	1310 nm DFB
05h	1550 nm DFB
06h	1310 nm EML
07h	1550 nm EML
08h	Others
09h	1490 nm DFB
0Ah	Copper cable unequalized
0Bh	Copper cable passive equalized
0Ch	Copper cable, near and far end limiting active equalizers
0Dh	Copper cable, far end limiting active equalizers
0Eh	Copper cable, near end limiting active equalizers
0Fh	Copper cable, linear active equalizers
10h-FFh	Reserved

8.3.15 Page 00h Checksum

The checksum is a one byte code that can be used to verify that the read-only static data on Page 00h is valid. The checksum code shall be the low order 8 bits of the arithmetic sum of all byte values from byte 128 to byte 221, inclusive.

8.3.16 Custom Info (non-volatile)

Bytes 223-255 are allocated in the non-volatile storage space for information provided by the original manufacturer of the module or the module reseller. This information persists across module reset and power cycle. The contents of this area are not defined by this specification.

8.4 Page 01h (Advertising)

Page 01h contains advertising fields that define properties that are unique to active modules and cable assemblies. The presence of Page 01h is advertised in bit 7 in Page 00h byte 2. All fields on Page 01h are read-only and static.

Table 8-25 Page 01h Overview

Byte	Size (bytes)	Name	Description
128-131	4	Module Firmware and Hardware revisions	
132-137	6	Supported link length	Supported lengths of various fiber media
138-139	2	Nominal Wavelength	
140-141	2	Wavelength Tolerance	
142-144	3	Implemented Memory Pages and Durations advertising	
145-154	10	Module Characteristics advertising	
155-156	2	Implemented Controls advertising	
157-158	2	Implemented Flags advertising	
159-160	2	Implemented Monitors advertising	
161-162	2	Implemented Signal Integrity Controls advertising	
163-166	4	CDB support advertising	
167-168	2	Additional Durations advertising	
169-175	7	Reserved	
176-190	15	Module Media Lane advertising	
191-222	32	Custom	
223-250	28	Extended Module Host-Media Interface Advertising options	
251-254	4	Reserved	
255	1	Checksum	Checksum of bytes 130-254[1]

Note 1: The firmware version bytes 128-129 are excluded from the checksum to allow module implementers to programmatically generate these fields and avoid requiring a memory map update when firmware is updated.

8.4.1 Module Inactive Firmware and Hardware Revisions

Table 8-26 describes the memory map locations for reporting module's inactive firmware and the module's hardware revisions. The finished module or cable assembly revision number shall be reported in the Vendor Revision Number field described in section 8.3.5

The module inactive firmware major and minor revisions shall be represented as numeric values. These two values shall not be included in the Page 01h checksum as these byte may change dynamically for modules that supports switching firmware version between multiple images during firmware upgrades. The inactive firmware is the alternate or backup firmware image that may reside on the module. These bytes have the same special encoding as the active firmware major and minor revisions (see section 8.2.8)

The module hardware major and minor revisions shall be represented as numeric values. These two values shall be included in the Page 01h checksum.

Table 8-26 Module Inactive Firmware and Hardware Revisions (Page 01h)

Byte	Bits	Name	Description	Type
128	7-0	Inactive Module firmware major revision	Numeric representation of inactive module firmware major revision	RO RQD
129	7-0	Inactive Module firmware minor revision	Numeric representation of inactive module firmware minor revision	RO RQD
130	7-0	Module hardware major revision	Numeric representation of module hardware major revision	RO RQD
131	7-0	Module hardware minor revision	Numeric representation of module hardware minor revision	RO RQD

8.4.2 Supported Link Length

These bytes define the maximum supported fiber media length for each type of fiber media at the maximum module-supported bit rate for active modules with a separable optical interface. Unsupported media types shall be populated with zeroes. Active optical cables shall populate the fields in this table with zeroes and instead report their actual length using the fields in Table 8-19.

Table 8-27 Supported Fiber Link Length (Page 01h)

Byte	Bits	Name	Description	Type
132	7-6	Length multiplier(SMF)	Link length multiplier for SMF fiber 00 = 0.1 (1 to 6.3 km) 01 = 1 (1 to 63 km) 10, 11 = reserved	RO RQD
	5-0	Base Length (SMF)	Base link length for SMF fiber. Must be multiplied by value in bits 7-6 to calculate actual link length in km.	
133	7-0	Length (OM5)	Link length supported for OM5 fiber, units of 2 m (2 to 510 m)	RO RQD
134	7-0	Length (OM4)	Link length supported for OM4 fiber, units of 2 m (2 to 510 m)	RO RQD
135	7-0	Length (OM3)	Link length supported for EBW 50/125 µm fiber (OM3), units of 2m (2 to 510 m)	RO RQD
136	7-0	Length (OM2)	Link length supported for 50/125 µm fiber (OM2), units of 1m (1 to 255 m)	RO RQD
137	7-0	Reserved		RORQD

The link length supported for SMF fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using single mode fiber. The supported link length is as specified in the SFF 8074i standard. The value is in units of kilometers.

The link length supported for OM5 fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 4700 MHz*km (850 nm) and 2470 MHz*km (953 nm) extended bandwidth 50 micron core multimode fiber. The value is in units of two meters.

The link length supported for OM4 fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 4700 MHz*km (850 nm) extended bandwidth 50 micron core multimode fiber. The value is in units of two meters.

The link length supported for OM3 fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 2000 MHz*km (850 nm) extended bandwidth 50 micron core multimode fiber. The value is in units of two meters.

The link length supported for OM2 fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 500 MHz*km (850 nm and 1310 nm) 50 micron multi-mode fiber. The value is in units of one meter.

8.4.3 Wavelength (Page 01h, Bytes 138 - 139, RO, RQD)

The wavelength field specifies the nominal transmitter output wavelength at room temperature; this is a 16-bit value with byte 138 as the high order byte and byte 139 as the low order byte. The laser wavelength value is equal to the 16-bit integer value of the wavelength in nm divided by 20 (units of 0.05nm). This resolution should be adequate to cover all relevant wavelengths yet provide enough resolution for all expected Applications. For accurate representation of controlled wavelength Applications, this value should represent the center of the guaranteed wavelength range.

8.4.4 Wavelength Tolerance (Page 01h, Bytes 140 - 141, RO, RQD)

The wavelength tolerance is the worst case +/- range of the transmitter output wavelength under all normal operating conditions; this is a 16-bit value with byte 140 as the high order byte and byte 141 as the low order byte. The laser wavelength tolerance is equal to the 16-bit integer value in nm divided by 200 (units of 0.005nm). Thus, the following two examples:

Example 1:

10GBASE-LR Wavelength Range = 1260 to 1355 nm
Nominal Wavelength in bytes 138 - 139 = 1307.5 nm.
Represented as INT (1307.5 nm * 20) = 26150 = 6626h
Wavelength Tolerance in bytes 140 - 141 = 47.5nm.
Represented as INT (47.5 nm * 200) = 9500 = 251Ch

Example 2:

ITU-T Grid Wavelength = 1534.25 nm with 0.236 nm Tolerance
Nominal Wavelength in bytes 138 - 139 = 1534.25 nm.
Represented as INT (1534.25 nm * 20) = 30685 = 77DDh
Wavelength Tolerance in bytes 140 - 141 = 0.236 nm.
Represented as INT (0.236 nm * 200) = 47 = 002Fh

8.4.5 Implemented Memory Pages and Durations Advertising

The fields in Table 8-28 advertise module implementation of optional management interface features.

The ModSelL wait time fields define the required setup time for the ModSelL signal after the host asserts a low level on ModSelL before the start of a two-wire serial bus transaction, and the required delay from completion of a two-wire serial bus transaction before the host can de-assert the ModSelL signal. For example, if the module wait time is 1.6 ms, the mantissa field (bits 4-0) will be 11001b and the exponent field (bits 7-5) will be 110b indicating six zeroes after the 11001b for a net result of 11001000000b or 1600 decimal.

Table 8-28 Implemented Management Interface Features Advertising (Page 01h)

Byte	Bit	Name	Description	Type
142	7	Reserved		RO RQD
	6	Versatile Diagnostic Monitoring	Pages 20h-2Fh implemented for versatile diagnostic monitoring	RO RQD
	5	Diagnostic pages implemented	Bank page 13h-14h implemented for diagnostic features	RO RQD
	4	reserved		
	3	reserved		
	2	Page 03h implemented	Indicates User page 03h implemented	
	1-0	Implemented Banks[1]	Indicates bank pages implemented for pages 10h-1Fh 00b=bank 0 implemented 01b=banks 0 and 1 implemented 10b=banks 0. 1. 2, 3 implemented 11b=reserved	
143	7-5	ModSelL wait time exponent	The ModSelL wait time value is the mantissa x 2^exponent expressed in micro-seconds. In other words, the mantissa field is shifted up by the number of bits indicated in the exponent field (time = mantissa << exponent)	RO Opt.
	4-0	ModSelL wait time mantissa		
144	7-4	DataPathDeinit_MaxDuration	Encoded maximum duration of the DataPathDeinit state (see Table 8-29)	RO RQD
	3-0	DataPathInit_MaxDuration	Encoded maximum duration of the DataPathInit state (see Table 8-29)	

Note 1: For module response to host attempts to write an invalid bank page combination see sections 8.2.11 and 8.2.12.

The DataPathInit_MaxDuration and DataPathDeinit_MaxDuration fields are defined so host implementers can determine when something has gone wrong in the module during these states, for example a module firmware hang up. These values should be selected to represent the worst-case durations of these two states, across all advertised Applications and combinations of data paths. See sections 6.3.2.3 and 6.3.2.5 for details of the DataPathInit and DataPathDeinit states, respectively.

Table 8-29 State Duration Encoding (Page 01h)

Encoding	Maximum State Duration
0000b	Maximum state duration is less than 1 ms
0001b	1 ms <= maximum state duration < 5 ms
0010b	5 ms <= maximum state duration < 10 ms
0011b	10 ms <= maximum state duration < 50 ms
0100b	50 ms <= maximum state duration < 100 ms
0101b	100 ms <= maximum state duration < 500 ms
0110b	500 ms <= maximum state duration < 1 s
0111b	1 s <= maximum state duration < 5 s
1000b	5 s <= maximum state duration < 10 s
1001b	10 s <= maximum state duration < 1 min
1010b	1 min <= maximum state duration < 5 min
1011b	5 min <= maximum state duration < 10 min
1100b	10 min <= maximum state duration < 50 min
1101b	Maximum state duration >= 50 min
1110b	Reserved
1111b	Reserved

8.4.6 Module Characteristics Advertising

The fields in Table 8-30 describe the characteristics of certain module properties. Some features may be optional. Advertisement of the implementation of optional features is in sections 8.4.7 through 8.4.10. A Tx synchronous group is defined as a Tx input lane or group of Tx input lanes sourced from the same clock domain. Two different Tx synchronous groups may be sourced from different clock domains. There may be a limit on the maximum permissible clock tolerance between two different Tx synchronous groups, as defined by the industry standard associated with a given application code. Refer to applicable industry standards.

A Tx synchronous group can contain one or more data paths, as long as the Tx lanes on all data paths are sourced from the same clock domain and the module takes measures to ensure that active data paths continue to operate undisturbed even as other data paths (and their associated Tx input lanes) are enabled/disabled by the host.

Table 8-30 Module Characteristics Advertising (Page 01h)

Byte	Bit	Name	Description	Type
145	7	Cooling implemented	0b=Uncooled transmitter device 1b=Cooled transmitter	RO RQD
	6-5	Tx input clock recovery capabilities	00b=module requires all Tx input lanes to be in a single Tx synchronous group 01b=module allows Tx input lanes 1-4 and 5-8 to be in separate Tx synchronous groups 10b=module allows Tx input lanes 1-2, 3-4, 5-6, 7-8 to be in separate Tx synchronous groups 11b=module allows each Tx input lane to be in a separate Tx synchronous group	RO RQD
	4-3	Reserved		RO
	2	Aux 3 Monitor type	1b=Aux 3 monitor is Vcc2 0b=Aux 3 monitor is Laser Temperature	RO Opt.
	1	Aux 2 Monitor type	1b=Aux 2 monitor is TEC current 0b=Aux 2 monitor is Laser Temperature	RO Opt.
	0	Aux 1 Monitor type	1b=Aux 1 monitor is TEC current 0b=Aux 1 monitor is reserved	RO Opt.
146	7-0	Maximum module temperature	Maximum allowed module case temperature 8-bit signed 2's complement value in 1 deg C increments. A value of all zeroes indicates not specified.	RO Opt.
147	7-0	Minimum module temperature	Minimum allowed module case temperature 8-bit signed 2's complement value in 1 deg C increments. A value of all zeroes indicates not specified.	RO Opt.
148	7-0	Propagation Delay MSB	Propagation delay of the non-separable AOC in multiples of 10 ns rounded to the nearest 10 ns. A value of all zeroes indicates not specified.	RO Opt.
149	7-0	Propagation Delay LSB		RO Opt.
150	7-0	Minimum operating voltage	Minimum supported module operating voltage, in 20 mV increments (0 - 5.1 V) A value of all zeroes indicates not specified.	RO Opt.
151	7	Detector type	0b=PIN detector 1b=APD detector	RO RQD
	6-5	Rx Output Eq type	00b=Peak-to-peak amplitude stays constant, or not implemented, or no information 01b=Steady-state amplitude stays constant 10b=Average of peak-to-peak and steady-state amplitude stays constant 11b=Reserved	

Byte	Bit	Name	Description	Type
	4	Rx Optical Power Measurement type	0b=OMA 1b=average power	
	3	Rx LOS type	0b=Rx LOS responds to OMA 1b=Rx LOS responds to Pave	
	2	Rx LOS fast mode implemented	0b=Rx LOS fast mode not implemented 1b=Rx LOS fast mode implemented Refer to form factor hardware specification for timing requirements	
	1	Tx Disable fast mode implemented	0b=Tx Disable fast mode not implemented 1b=Tx Disable fast mode implemented Refer to form factor hardware specification for timing requirements	
	0	Module-Wide Tx Disable	0b=Tx Disable implemented per lane 1b=Any Tx Disable control bit being set disables all Tx lanes	
152	7-0	Per lane CDR Power saved	Minimum power consumption saved per CDR per lane when placed in CDR bypass in multiples of 0.01 W rounded up to the next whole multiple of 0.01 W	RO Opt.
153	7	Rx Output Amplitude code 0011b implemented[1]	0b=Amplitude code 0011b not implemented 1b=Amplitude code 0011b implemented	RO Opt.
	6	Rx Output Amplitude code 0010b implemented[1]	0b=Amplitude code 0010b not implemented 1b=Amplitude code 0010b implemented	
	5	Rx Output Amplitude code 0001b implemented[1]	0b=Amplitude code 0001b not implemented 1b=Amplitude code 0001b implemented	
	4	Rx Output Amplitude code 0000b implemented[1]	0b=Amplitude code 0000b not implemented 1b=Amplitude code 0000b implemented	
	3-0	Max Tx Input Eq	Maximum supported value of the Tx Input Equalization control for manual/fixed programming. (see section 6.2.4.1)	
154	7-4	Max Rx Output Eq Post-cursor	Maximum supported value of the Rx Output Eq Post-cursor control. (see section 6.2.4.2)	RO Opt.
	3-0	Max Rx Output Eq Pre-cursor	Maximum supported value of the Rx Output Eq Pre-cursor control (see section 6.2.4.2)	

Note 1: See Table 6-6

8.4.7 Implemented Controls Advertisement

Table 8-31 describes implemented module and lane controls.

Table 8-31 Implemented Controls Advertisement (Page 01h)

Byte	Bit	Name	Description	Type
155	7	Wavelength control implemented	0b=No wavelength control 1b=Active wavelength control implemented	RO RQD
	6	Tunable transmitter implemented	0b=Transmitter not tunable 1b=Transmitter tunable (page 04h and bank page 12h shall be implemented)	
	5-4	Tx Squelch implemented	00b=Tx Squelch not implemented 01b=Tx Squelch reduces OMA 10b=Tx Squelch reduces Pave 11b=User control, both OMA and Pave squelch supported. (see Table 8-7)	
	3	Tx Force Squelch implemented	0b=Tx Force Squelch not implemented 1b=Tx Force Squelch implemented	
	2	Tx Squelch Disable implemented	0b=Tx Squelch Disable not implemented	

Byte	Bit	Name	Description	Type
			1b=Tx Squelch Disable implemented	
	1	Tx Disable implemented	0b=Tx Disable not implemented 1b=Tx Disable implemented	
	0	Tx Polarity Flip implemented	0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented	
156	7-3	Reserved		RO RQD
	2	Rx Squelch Disable implemented	0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented	RO RQD
	1	Rx Disable implemented	0b=Rx Disable not implemented 1b=Rx Disable implemented	
	0	Rx Polarity Flip implemented	0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented	

8.4.8 Implemented Flags Advertisement

Table 8-32 describes implemented module and lane flags.

Table 8-32 Implemented Flags Advertisement (Page 01h)

Byte	Bit	Name	Description	Type
157	7-4	Reserved		RO RQD
	3	Tx Adaptive Input Eq Failflag implemented	0b=Tx Adaptive Input Eq Fail flag not implemented 1b=Tx Adaptive Input Eq Fail flag implemented	RO RQD
	2	Tx CDR LOL flag implemented	0b=Tx CDR Loss of Lock flag not implemented 1b=Tx CDR Loss of Lock flag implemented	
	1	Tx LOS flag implemented	0b=Tx Loss of Signal flag not implemented 1b=Tx Loss of Signal flag implemented	
	0	Tx Fault flag implemented	0b=Tx Fault flag not implemented 1b=Tx Fault flag implemented	
158	7-3	Reserved		RO RQD
	2	Rx LOL flag implemented	0b=Rx CDR Loss of Lock flag not implemented 1b=Rx CDR Loss of Lock flag implemented	RO RQD
	1	Rx LOS flag implemented	0b=Rx Loss of Signal flag not implemented 1b=Rx Loss of Signal flag implemented	
	0	Reserved		RO

8.4.9 Implemented Monitors Advertisement

Table 8-33 describes implemented module and lane monitors.

Table 8-33 Implemented Monitors Advertisement (Page 01h)

Byte	Bit	Name	Description	Type
159	7-6	Reserved		RO RQD
	5	Custom monitor implemented	0b=Custom monitor not implemented 1b=Custom monitor implemented	RO RQD
	4	Aux 3 monitor implemented	0b=Aux 3 monitor not implemented 1b=Aux 3 monitor implemented	
	3	Aux 2 monitor implemented	0b=Aux 2 monitor not implemented 1b=Aux 2 monitor implemented	

Byte	Bit	Name	Description	Type
	2	Aux 1 monitor implemented	0b=Aux 1 monitor not implemented 1b=Aux 1 monitor implemented	
	1	Internal 3.3 Volts monitor implemented	0b=Internal 3.3 V monitor not implemented 1b=Internal 3.3 V monitor implemented	
	0	Temperature monitor implemented	0b=Temperature monitor not implemented 1b=Temperature monitor implemented	
160	7-5	Reserved		RO RQD
	4-3	Tx Bias current measurement and threshold multiplier	Multiplier for 2uA Bias current increment used in Tx Bias current monitor and threshold registers (see Table 8-42 and Table 8-62) 00b=multiply x1 01b=multiply x2 10b=multiply x4 11b=reserved	
	2	Rx Optical Input Power monitor implemented	0b=Rx Optical Input Power monitor not implemented 1b=Rx Optical Input Power monitor implemented	
	1	Tx Output Optical Power monitor implemented	0b=Tx Output Optical Power monitor not implemented 1b=Tx Output Optical Power monitor implemented	
	0	Tx Bias monitor implemented	0b=Tx Bias monitor not implemented 1b=Tx Bias monitor implemented	

8.4.10 Implemented Signal Integrity Controls Advertisement

Table 8-34 describes the advertisement of implemented signal integrity controls.

Table 8-34 Implemented Signal Integrity Controls Advertisement(Page 01h)

Byte	Bit	Name	Description	Type
161	7	Reserved		RO RQD
	6-5	Tx Input Eq Store/Recall buffer count	00b=Tx Input Eq Store/Recall not implemented 01b=Tx Input Eq Store/Recall buffer count=1 10b=Tx Input Eq Store/Recall buffer count=2 11b=reserved	RO RQD
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
	2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	7-6	Reserved		RO RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Page 10h	RO RQD
	4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
	2	Rx Output Amplitude control	0b=Rx Output Amplitude control not implemented	

Byte	Bit	Name	Description	Type
		implemented	1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	

8.4.11 CDB Support Advertisement

Table 8-35 describes the support of the Command Data Block (CDB) and some high-level features therein. Support for specific CDB commands is advertised through the CDB commands shown in Table 10-1. See section 7.2 for more details on CDB usage.

Table 8-35 CDB Advertisement (Page 01h)

Byte	Bit	Name	Description	Type
163	7-6	CDB implemented	00b=CDB not implemented 01b=Only one instance of CDB implemented. In Pages 9Fh and A0h-AFh, Bank 0 only supported 10b=Two instances of CDB implemented. In Pages 9Fh and A0h-AFh, Bank 0 and 1 supported 11b=Reserved If coded 01b implementation of Byte 8 bit 6 (L-CDB block 1 command complete) flag and associated mask bit (Byte 31 bit 6) is required. If coded 10b implementation of Byte 8 bits 7-6 (L-CDB block 1 and 2 command complete) flags and associated mask bits (Byte 31 bits 7-6) is required.	RO RQD
	5	CDB background operation implemented	0b=Background CDB operation not implemented. The module may NACK after CDB command is triggered, until the command is complete. 1b=Background CDB operation implemented	RO RQD
	4	CDB Auto Paging implemented	When the memory map address pointer advances past the end of an EPL CDB page, the page number will automatically increment and the memory map address pointer will automatically wrap to 128 0b=Auto Paging not implemented 1b=Auto Paging and Auto page wrap implemented	RO RQD
	3-0	Number of EPL Pages implemented	This field defines which EPL pages are implemented in the module and is encoded as follows 0=Pages A0h-AFh not implemented 1=Page A0h implemented, A1h-AFh not implemented 2=Page A0h-A1h implemented, A2h-AFh not implemented 3=Page A0h-A2h implemented, A3h-AFh not implemented 4=Page A0h-A3h implemented, A4h-AFh not implemented 5=Page A0h-A7h implemented, A8h-AFh not implemented 6=Page A0h-ABh implemented, ACh-AFh not implemented 7=Page A0h-AFh implemented The module shall support host reads from and writes to all implemented EPL pages. The behavior of these pages is dependent on the associated CDB command. The advertised Number of EPL Pages Implemented shall be	RO RQD

Byte	Bit	Name	Description	Type
			consistent with the pages required for each supported CDB command.	
164	7-0	CDB Max TWI Bytes per write transaction	This specification limits the length of TWI write transactions to 8 bytes. This field allows the module to advertise support for longer TWI write transactions, but on CDB pages 9Fh-AFh only. The encoding of this field is as follows: CdbMaxTWIWriteBytes = (Byte 164+1) * 8 A value of 0 indicates that a maximum write length of 8 bytes is permitted. A value of 255 indicates a maximum write length of 2048 bytes is permitted. If the TWI write transaction from the host is longer than the advertised supported max length, the module may ignore bytes that are written beyond the advertised supported max length.	RO RQD
165	7	CDB command processing option	1b: CDB commands are processed on STOP bit when CMD 128/129 registers are within the write I2C transaction 0b: CDB commands are processed on a write to Byte 129 of Page 9F.	
	6-5	Reserved		
	4-0	CDB commands tNACK time	Denotes tNACK for CDB commands if above 80ms using values of 0-31b. Encoding of tNACK for CDB is this register value*160 ms. The maximum supported tNACK is 4960 ms (Value = 31). This value is ignored when Byte 166 bit 7 is 0b.	
166	7	CDB tNACK time indicator	0b: Indicates that tNACK in bits 6-0 also applies to CDB Generic commands. 1b: Indicates that tNACK in bits 6-0 does not apply to CDB Generic commands. CDB tNACK may be equal to 80 ms or as advertised in Byte 165 Bits 4-0.	
	6-0	Maximum tNACK time	tNACK = (80 - XX) ms. XX is the value of this register in ms. A value of 000 0000b (0) defines modules maximum tNACK of 80 ms. Values of XX>= 80 will be interpreted as having tNACK of 0.	

The CDB Implemented field in page 01h, byte 163, bits 7-6 defines if CDB is supported. If CDB is implemented, this field identifies how many concurrent CDB commands, called CDB instances, are supported in the module. Each CDB instance is associated with a bank number. All CDB instances are expected to behave identically and support the same set of CDB commands. Module support for multiple CDB instances can be useful when long-duration CDB commands are supported, such as firmware update.

The CDB Background Operation Implemented field in byte 163, bit 5 defines if the host may perform other TWI transactions while a CDB command is being executed. If this bit is 0b, the module will NACK while a CDB command is being executed until the command is completed, consistent with the behaviors described in section 5.4.5. If this bit is 1b, the module will NACK until the CDB command is captured. After the command is captured, the module will again respond to TWI transactions. When CDB Background Operation is supported, the host may read the CDB Status field to determine the status of in-progress CDB commands (see Table 8-9). While a CDB Command is being executed in the background, the module shall ensure that any flash writes to code areas do not affect other host interactions with the module that may be occurring in the foreground.

The CDB Auto Paging Implemented (Byte 163, bit 4), Number of EPL pages Implemented (Byte 163, bits 3-0), and CDB Max TWI Bytes Per Write Transaction (Page 01h, Byte 164) fields are interrelated. The module uses

these fields to advertise the capabilities of the module. There are some combinations of these fields that should be avoided and some combinations that require further clarification of expected module behaviors. These combinations are described in Table 8-36, below.

Table 8-36 Overview of CDB advertising combinations

CDB Auto Paging impl. (Page 01h, Byte 163, bit 4)	Number of EPL pages impl. (Page 01h, Byte 163, bits 3-0)	CDB Max TWI Bytes per write transaction (Page 01h, Byte 164)	Description
0	Any	<= 128 bytes	This combination is a valid combination and may be advertised. While the host may write up to CDB Max TWI Bytes per write transaction, the host should be careful about writing past the end of the page, since auto paging is not implemented.
0	Any	> 128 bytes	This combination is invalid and should not be advertised, because module behavior for TWI write transactions > 128 bytes is undefined
1	0 or 1 pages	Any	This combination is invalid and should not be advertised, because auto paging is only applicable to multi-page EPL implementations.
1	>= 2 pages	Any	This combination is a valid combination and may be advertised. Since Auto Paging is supported, a TWI write past address 255 will automatically increment the page number and wrap the write address to byte 128. If the host writes past the last implemented EPL page, the page wraps to A0h. If a “page wrap around occurs” the host can no longer read-back the data to compare. The host may use the Auto Paging feature to “stream” data into the module without the overhead of managing page changes.

As an example, the module may advertise a 4 in the Number of EPL Pages Implemented field, indicating support for pages A0-A3h only, but also advertise 255 in the CDB Max TWI Bytes Per Write Transaction field, indicating support for up to 2048 byte writes. This combination is a valid combination. However, since the Max TWI Bytes per write transaction is larger than the number of bytes that can be supported by unique pages, the data written will be accepted by the module but the host may not be able to uniquely read back the data written. To allow for unique read-back of data, the module shall advertise support of a matching number of EPL page bytes and maximum TWI write transaction size.

8.4.12 Additional Durations Advertising

The fields in Table 8-37 advertise module implementation of optional management interface features.

Table 8-37 Additional State Machine Durations Advertising (Page 01h)

Byte	Bit	Name	Description	Type
167	7-4	ModulePwrDn_MaxDuration	Encoded maximum duration of the ModulePwrDn state (see Table 8-29)	RO RQD
	3-0	ModulePwrUp_MaxDuration	Encoded maximum duration of the ModulePwrUp state (see Table 8-29)	
168	7-4	DataPathTxTurnOff_MaxDuration	Encoded maximum duration of the DataPathTxTurnOff state (see Table 8-29)	RO RQD

	3-0	DataPathTxTurnOn_MaxDuration	Encoded maximum duration of the DataPathTxTurnOn state (see Table 8-29)	

These *_MaxDuration fields are defined so host implementers can determine when something has gone wrong in the module during these states, for example a module firmware hang up. These values should be selected to represent the worst-case durations of the applicable state, across all supported configurations. See sections 6.3.1.8 and 6.3.1.10 for details of the ModulePwrUp and ModulePwrDn states and sections 6.3.2.6 and 6.3.2.8 for details of the DataPathTxTurnOn and DataPathTxTurnOff states.

8.4.13 Media Lane Assignment Options Advertising

Each Application descriptor comprises five bytes to advertise an Application, as described in section 6.2.1.1.

The first four bytes are defined in Table 8-13 or Table 8-39. The fifth byte is defined here in Table 8-38. Both parts of the application descriptor are linked by the descriptor number known as ApSel Code .

Table 8-38 Media Lane Assignment Advertising (Page 01h)

Byte	Bits	Name	Description	Type
176	7-0	Media Lane Assignment Options, ApSel 0001b	Coded 1 if the Application is allowed to begin on a given media lane. Bits 0-7 correspond to Host Lanes 1-8. In multi-lane Applications each instance of an Application shall use contiguous media lane numbers. If multiple instances of a single Application are allowed each starting point is identified. If multiple instances are advertised, all instance must be supported concurrently. (See section 6.2.1)	RO RQD
177	7-0	Media Lane Assignment Options, ApSel 0010b		
178	7-0	Media Lane Assignment Options, ApSel 0011b		
179	7-0	Media Lane Assignment Options, ApSel 0100b		
180	7-0	Media Lane Assignment Options, ApSel 0101b		
181	7-0	Media Lane Assignment Options, ApSel 0110b		
182	7-0	Media Lane Assignment Options, ApSel 0111b		
183	7-0	Media Lane Assignment Options, ApSel 1000b		
184	7-0	Media Lane Assignment Options, ApSel 1001b		
185	7-0	Media Lane Assignment Options, ApSel 1010b		
186	7-0	Media Lane Assignment Options, ApSel 1011b		
187	7-0	Media Lane Assignment Options, ApSel 1100b		
188	7-0	Media Lane Assignment Options, ApSel 1101b		
189	7-0	Media Lane Assignment Options, ApSel 1110b		
190	7-0	Media Lane Assignment Options, ApSel 1111b		

8.4.14 Additional Application Advertising

Table 8-39 adds up to seven additional Application descriptors to the eight Application descriptors in Table 8-13.

See section 6.2.1.1 for Application advertising methodology and section 8.2.9 for information about the descriptor and the descriptor table format.

The Host Electrical Interface ID field of the first unused descriptor in Table 8-39 shall have a value of FFh, indicating the end of the list of Application descriptors.

Table 8-39 Additional Application Advertising Fields (Page 01h)

Byte	Bits	ApSel Code	Name	Description	Type
223	7-0		Host Electrical Interface ID	ID from SFF-8024 Coded FFh if first unused ApSel code	RO Opt.
224	7-0		Module Media Interface ID	ID from table selected by Byte 85 (see Table 8-12)	
225	7-4		Host Lane Count	0000b=lane count defined by interface code 0001b=1 lane 0010b=2 lanes ... 1000b=8 lanes 1001b-1111b=reserved	
	3-0	1001b	Media Lane Count		
226	7-0		Host Lane Assignment Options (See Table 8-38 for Media Lane Assignment Options)	Bits 0-7 form a bit map and correspond to Host Lanes 1-8. A bit is coded 1 if the Application is allowed to begin on the corresponding host lane. Refer to section 6.2.1.1 for details.	
227	7-0		Host Electrical Interface ID	See ApSel Code 1001b	RO Opt.
228	7-0		Module Media Interface ID	See ApSel Code 1001b	
229	7-4	1010b	Host Lane Count	See ApSel Code 1001b	
	3-0		Media Lane Count		
230	7-0		Host Lane Assignment Options	See ApSel Code 1001b	
231	7-0		Host Electrical Interface ID	See ApSel Code 1001b	RO Opt.
232	7-0		Module Media Interface ID	See ApSel Code 1001b	
233	7-4	1011b	Host Lane Count	See ApSel Code 1001b	
	3-0		Media Lane Count		
234	7-0		Host Lane Assignment Options	See ApSel Code 1001b	
235	7-0		Host Electrical Interface ID	See ApSel Code 1001b	RO Opt.
236	7-0		Module Media Interface ID	See ApSel Code 1001b	
237	7-4	1100b	Host Lane Count	See ApSel Code 1001b	
	3-0		Media Lane Count		
238	7-0		Host Lane Assignment Options	See ApSel Code 1001b	
239	7-0		Host Electrical Interface ID	See ApSel Code 1001b	RO Opt.
240	7-0		Module Media Interface ID	See ApSel Code 1001b	
241	7-4	1101b	Host Lane Count	See ApSel Code 1001b	
	3-0		Media Lane Count		
242	7-0		Host Lane Assignment Options	See ApSel Code 1001b	
243	7-0		Host Electrical Interface ID	See ApSel Code 1001b	RO Opt.
244	7-0		Module Media Interface ID	See ApSel Code 1001b	
245	7-4	1110b	Host Lane Count	See ApSel Code 1001b	
	3-0		Media Lane Count		
246	7-0		Host Lane Assignment Options	See ApSel Code 1001b	
247	7-0		Host Electrical Interface ID	See ApSel Code 1001b	RO Opt.
248	7-0		Module Media Interface ID	See ApSel Code 1001b	
249	7-4	1111b	Host Lane Count	See ApSel Code 1001b	
	3-0		Media Lane Count		
250	7-0		Host Lane Assignment Options	See ApSel Code 1001b	

8.4.15 Checksum (Upper Page 01h, Byte 255, RO RQD)

The checksum is a one byte code that can be used to verify that the read-only static data on Page 01h is valid. The checksum code shall be the low order 8 bits of the arithmetic sum of all byte values from byte 130 to byte 254, inclusive. Note that the module firmware revision in bytes 128 and 129 is not included in the checksum.

8.5 Page 02h (Module and Lane Thresholds)

Page 02h contains the module-defined thresholds for module-level and lane-specific monitors. The presence of Page 02h is advertised in bit 7 in Page 00h byte 2. All fields on Page 02h are read-only and static.

Table 8-40 Page 02h Overview

Byte	Size (bytes)	Name	Description
128-175	48	Module-level monitor thresholds	
176-199	24	Lane-specific monitor thresholds	
200-229	30	Reserved	
230-254	25	Custom	
255	1	Checksum	Covers bytes 128-254

8.5.1 Module-Level Monitor Thresholds

The following thresholds are provided by the module to inform the host of the monitor levels where alarms and warnings will be triggered.

Table 8-41 Module-Level Monitor Thresholds (Page 02h)

Byte	Bit	Name	Description	Type
128	7-0	Temperature monitor high alarm threshold MSB	Thresholds for internally measured temperature monitor: signed 2's complement in 1/256 degree Celsius increments	RO Opt.
129	7-0	Temperature monitor high alarm threshold LSB		
130	7-0	Temperature monitor low alarm threshold MSB		
131	7-0	Temperature monitor low alarm threshold LSB		
132	7-0	Temperature monitor high warning threshold MSB		
133	7-0	Temperature monitor high warning threshold LSB		
134	7-0	Temperature monitor low warning threshold MSB		
135	7-0	Temperature monitor low warning threshold LSB		
136	7-0	Supply 3.3-volt monitor high alarm threshold MSB	Thresholds for internally measured 3.3 volt input supply voltage: in 100 µV increments	RO Opt.
137	7-0	Supply 3.3-volt monitor high alarm threshold LSB		
138	7-0	Supply 3.3-volt monitor low alarm threshold MSB		
139	7-0	Supply 3.3-volt monitor low alarm threshold LSB		
140	7-0	Supply 3.3-volt monitor high warning threshold MSB		
141	7-0	Supply 3.3-volt monitor high warning threshold LSB		
142	7-0	Supply 3.3-volt monitor low warning threshold MSB		

Byte	Bit	Name	Description	Type
143	7-0	Supply 3.3-volt monitor low warning threshold LSB		
144	7-0	Aux 1 monitor high alarm threshold MSB	Thresholds for TEC Current or Reserved monitor TEC Current: signed 2's complement in 100/32767% increments of maximum TEC current +32767 is max TEC current (100%) – Max Heating -32767 is min TEC current (100%) – Max Cooling	RO Opt.
145	7-0	Aux 1 monitor high alarm threshold LSB		
146	7-0	Aux 1 monitor low alarm threshold MSB		
147	7-0	Aux 1 monitor low alarm threshold LSB		
148	7-0	Aux 1 monitor high warning threshold MSB		
149	7-0	Aux 1 monitor high warning threshold LSB		
150	7-0	Aux 1 monitor low warning threshold MSB		
151	7-0	Aux 1 monitor low warning threshold LSB		
152	7-0	Aux 2 monitor high alarm threshold MSB	Thresholds for TEC Current or Laser Temperature monitor TEC Current: signed 2's complement in 100/32767% increments of maximum TEC current+32767 is max TEC current (100%) – Max Heating -32767 is min TEC current (100%) – Max Cooling Laser Temperature: signed 2's complement in 1/256 degree Celsius increments	RO Opt.
153	7-0	Aux 2 monitor high alarm threshold LSB		
154	7-0	Aux 2 monitor low alarm threshold MSB		
155	7-0	Aux 2 monitor low alarm threshold LSB		
156	7-0	Aux 2 monitor high warning threshold MSB		
157	7-0	Aux 2 monitor high warning threshold LSB		
158	7-0	Aux 2 monitor low warning threshold MSB		
159	7-0	Aux 2 monitor low warning threshold LSB		
160	7-0	Aux 3 monitor high alarm threshold MSB	Thresholds for Laser Temperature or additional supply voltage monitor Laser Temperature: signed 2's complement in 1/256 degree Celsius increments NOTE: Laser Temp can be below 0 if uncooled or in Tx Disable. Additional supply voltage monitor: in 100 µV increments	RO Opt.
161	7-0	Aux 3 monitor high alarm threshold LSB		
162	7-0	Aux 3 monitor low alarm threshold MSB		
163	7-0	Aux 3 monitor low alarm threshold LSB		
164	7-0	Aux 3 monitor high warning threshold MSB		
165	7-0	Aux 3 monitor high warning threshold LSB		
166	7-0	Aux 3 monitor low warning threshold MSB		
167	7-0	Aux 3 monitor low warning threshold LSB		
168	7-0	Custom monitor high alarm threshold MSB	Custom monitor: signed or unsigned 16 bit value	RO Opt.
169	7-0	Custom monitor high alarm		

Byte	Bit	Name	Description	Type
		threshold LSB		
170	7-0	Custom monitor low alarm threshold MSB		
171	7-0	Custom monitor low alarm threshold LSB		
172	7-0	Custom monitor high warning threshold MSB		
173	7-0	Custom monitor high warning threshold LSB		
174	7-0	Custom monitor low warning threshold MSB		
175	7-0	Custom monitor low warning threshold LSB		

8.5.2 Lane-specific Monitor Thresholds

The following thresholds are provided by the module to inform the host of the monitor levels where alarms and warnings will be triggered.

Table 8-42 Lane-specific Monitor Thresholds (Page 02h, active modules only)

Byte	Bit	Name	Description	Type
176	7-0	Tx optical power monitor high alarm threshold MSB	Threshold for Tx optical power monitor: unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm) See section 8.8.3 for monitor details including accuracy	RO Opt.
177	7-0	Tx optical power high alarm threshold LSB		
178	7-0	Tx optical power low alarm threshold MSB		
179	7-0	Tx optical power low alarm threshold LSB		
180	7-0	Tx optical power high warning threshold MSB		
181	7-0	Tx optical power high warning threshold LSB		
182	7-0	Tx optical power low warning threshold MSB		
183	7-0	Tx optical power low warning threshold LSB		
184	7-0	Tx bias current monitor high alarm threshold MSB	Threshold for Tx bias monitor: unsigned integer in 2 uA increments, times the multiplier from Table 8-33. See section 8.8.3 for monitor details including accuracy	RO Opt.
185	7-0	Tx bias current high alarm threshold LSB		
186	7-0	Tx bias current low alarm threshold MSB		
187	7-0	Tx bias current low alarm threshold LSB		
188	7-0	Tx bias current high warning threshold MSB		
189	7-0	Tx bias current high warning threshold LSB		
190	7-0	Tx bias current low warning threshold MSB		
191	7-0	Tx bias current low warning threshold LSB		
192	7-0	Rx optical power monitor high alarm threshold MSB	Threshold for Rx optical power monitor: unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm) See section 8.8.3 for accuracy.	RO Opt.
193	7-0	Rx optical power high alarm threshold LSB		
194	7-0	Rx optical power low alarm threshold MSB		
195	7-0	Rx optical power low alarm threshold LSB		
196	7-0	Rx optical power high warning threshold MSB		
197	7-0	Rx optical power high warning threshold LSB		
198	7-0	Rx optical power low warning threshold MSB		
199	7-0	Rx optical power low warning threshold LSB		

8.5.3 Checksum (Page 02h, Byte 255, RO RQD)

The checksum code is a one-byte code that can be used to verify that the device property information in the module is valid. The checksum code shall be the low order 8 bits of the arithmetic sum of all byte values from byte 128 to byte 254, inclusive.

8.6 Laser Capabilities Advertising (Page 04h, Optional)

The memory map page 04h is used for advertising laser capabilities for tunable lasers. These capabilities are defined at a module level.

If Page 01h Byte 155 bit 6 is set to 1 (see Table 8-31), then this page is required to be supported.

Details for Bytes 128/129 are shown in Table 8-42. The 'n' in this table is the 16-bit signed channel number that is referred to in the highest/lowest supported channel numbers in page 04h. It is also the channel number to be used to tune the laser in page 12h.

Table 8-43 Laser capabilities for tunable lasers (Page 04h)

Byte	Bits	Name	Description	Type
128	7	75 GHz Grid Supported	Indicates whether the module supports channel-based tuning on 75 GHz grid. In this case, the tuning parameter n is defined as: Frequency = 193.1 + n × 0.025, where n must be divisible by 3. 0b = 75 GHz Grid not supported 1b = 75 GHz Grid supported n is the 16-bit signed channel number that is referred to in the highest/lowest supported channel numbers in page 04h	RO OPT.
	6	33 GHz Grid Supported	Indicates whether the module supports channel-based tuning on 33 GHz grid. In this case, the tuning parameter n is defined as: Frequency = 193.1 + n/3 × 0.1. 0b = 33 GHz Grid not supported 1b = 33 GHz Grid supported	RO OPT.
	5	100 GHz Grid Supported	Indicates whether the module supports channel-based tuning on 100 GHz grid. In this case, the tuning parameter n is defined as: Frequency = 193.1 + n × 0.1. 0b = 100 GHz Grid not supported 1b = 100 GHz Grid supported	RO OPT.
	4	50 GHz Grid Supported	Indicates whether the module supports channel-based tuning on 50 GHz grid. In this case, the tuning parameter n is defined as: Frequency = 193.1 + n × 0.05. 0b = 50 GHz Grid not supported 1b = 50 GHz Grid supported	RO OPT.
	3	25 GHz Grid Supported	Indicates whether the module supports channel-based tuning on 25 GHz grid. In this case, the tuning parameter n is defined as: Frequency 193.1 + n × 0.025. 0b = 25 GHz Grid not supported 1b = 25 GHz Grid supported	RO OPT.
	2	12.5 GHz Grid Supported	Indicates whether the module supports channel-based tuning on 12.5 GHz grid. In this case, the tuning parameter n is defined as: Frequency = 193.1 + n × 0.0125. 0b = 12.5 GHz Grid not supported 1b = 12.5 GHz Grid supported	RO OPT.
	1	6.25 GHz Grid Supported	Indicates whether the module supports channel-based tuning on 62.5 GHz grid. In this case, the tuning parameter n is defined as: Frequency = 193.1 + n × 0.00625. 0b = 6.25 GHz Grid not supported 1b = 6.25 GHz Grid supported	RO OPT.
	0	3.125 GHz Grid Supported	Indicates whether the module supports channel-based tuning on 3.125 GHz grid. In this case, the tuning parameter n is	RO OPT.

Byte	Bits	Name	Description	Type
			defined as: Frequency = 193.1 + n × 0.003125. 0b = 3.125 GHz Grid not supported 1b = 3.125 GHz Grid supported	
129	7	Fine tuning support	Indicates whether the module supports fine-tuning of laser frequency. 0b = module does not support fine-tuning 1b = module supports fine-tuning	RO OPT.
	6-0	Reserved	Reserved for future channel spacing advertisements	RO OPT.
130-131	7-0	3.125 GHz Grid Low Channel	Lowest supported n for 3.125 GHz spacing (16-bit signed)	RO OPT.
132-133	7-0	3.125 GHz Grid High Channel	Highest supported n for 3.125 GHz spacing (16-bit signed)	RO OPT.
134-135	7-0	6.25 GHz Grid Low Channel	Lowest supported n for 6.25 GHz spacing (16-bit signed)	RO OPT.
136-137	7-0	6.25 GHz Grid High Channel	Highest supported n for 6.25 GHz spacing (16-bit signed)	RO OPT.
138-139	7-0	12.5 GHz Grid Low Channel	Lowest supported n for 12.5 GHz spacing (16-bit signed)	RO OPT.
140-141	7-0	12.5 GHz Grid High Channel	Highest supported n for 12.5 GHz spacing (16-bit signed)	RO OPT.
142-143	7-0	25 GHz Grid Low Channel	Lowest supported n for 25 GHz spacing (16-bit signed)	RO OPT.
144-145	7-0	25 GHz Grid High Channel	Highest supported n for 25 GHz spacing (16-bit signed)	RO OPT.
146-147	7-0	50 GHz Grid Low Channel	Lowest supported n for 50 GHz spacing (16-bit signed)	RO OPT.
148-149	7-0	50 GHz Grid High Channel	Highest supported n for 50 GHz spacing (16-bit signed)	RO OPT.
150-151	7-0	100 GHz Grid Low Channel	Lowest supported n for 100 GHz spacing (16-bit signed)	RO OPT.
152-153	7-0	100 GHz Grid High Channel	Highest supported n for 100 GHz spacing (16-bit signed)	RO OPT.
154-155	7-0	33 GHz Grid Low Channel	Lowest supported n for 33 GHz spacing (16-bit signed)	RO OPT.
156-157	7-0	33 GHz Grid High Channel	Highest supported n for 33 GHz spacing (16-bit signed)	RO OPT.
158-159	7-0	75 GHz Grid Low Channel	Lowest supported n for 75 GHz spacing (16-bit signed)	RO OPT.
160-161	7-0	75 GHz Grid High Channel	Highest supported n for 75 GHz spacing (16-bit signed)	RO OPT.
162-189	7-0	Reserved	Reserved for future channel spacing support	RO OPT.
190-191	7-0	Fine-tuning resolution	Fine-tuning resolution, 16-bit unsigned in increments of 0.001 GHz	RO OPT.
192-193	7-0	Fine-tuning Low Offset	Signed 16-bit lowest fine-tuning offset, 16-bit signed value with resolution of 0.001 GHz (RO)	RO OPT.
194-195	7-0	Fine-tuning High Offset	Signed 16-bit highest fine-tuning offset, 16-bit signed in increments of 0.001 GHz (RO)	RO OPT.
196	7	Lane Programmable Output Power Supported	Indicates Lane support for programmable output power. 0b = Programmable output power not supported 1b = Programmable output power supported	RO OPT.

Byte	Bits	Name	Description	Type
	6-0	Reserved		
197	7-0	Reserved	Reserved	RO
198-199	7-0	Min. Prog. Output Power	Minimum Programmable Output Power, 16-bit signed value in increment of 0.01 dBm.	RO Opt.
200-201	7-0	Max. Prog. Output Power	Maximum Programmable Output Power, 16-bit signed value in increments of 0.01 dBm	RO Opt.
202-255	7-0	Reserved		RO

8.7 Page 10h (Lane and Data Path Control)

The upper memory map page 10h is a banked page that contains lane dynamic control bytes. The presence of Page 10h is advertised in bit 7 in Page 00h byte 2. Upper page 10h is subdivided into several areas as illustrated in the following table:

Table 8-44 Page 10h Overview

Byte	Size (bytes)	Name	Description
128	1	DataPathDeinit	Data Pathcontrol bits for each lane, controls Data Path State machine
129-142	14	Lane-Specific Control	Fields to control lane attributes independent of the Data Path State machine or control sets
143-177	35	Staged Control Set 0	Fields to configure the selected Application Code and signal integrity settings
178-212	35	Staged Control Set 1	Fields to configure the selected Application Code and signal integrity settings
213-231	19	Lane-Specific Flag Masks	
232-239	8	Reserved	
240-255	16	Custom	

8.7.1 Data Path Initialization Control

The DataPathDeinit byte controls the initialization of the lanes in a configured data path This field is ignored when the Module State is not ModuleReady.

The DataPathDeinit bits associated with all lanes in a single data path shall always have the same value. When the Module State is ModuleReady, the data path associated with lanes whose DataPathDeinit bits are set to 0 will transition to the DataPathInit state and begin the initialization process. Refer to section 6.3.2 for details about the Data Path State Machine. The host may deinitialize data paths by setting the appropriate bits to 1. Host implementers should note that, without host intervention, all data paths will begin initializing when the Module State reaches ModuleReady. This auto-initialization behavior can be prevented by writing a 1 to all DataPathDeinit bits when the module is in the ModuleLowPwr state.

Multiple data paths may be initialized or deinitialized at the same time.

The number of lanes in a data path is defined by the selected ApSel Code in the Active Set (see Table 8-65). Refer to section 6.2.1.1 for details on ApSel Codes and section 6.2.3 for details on Control Sets.

Table 8-45 Data Path initialization control (Page 10h)

Byte	Bit	Name	Description	Type
128	7	DataPathDeinit Host Lane 8	Data Path initialization control for host lane 8 0b=Initialize the data path associated with host lane 8 1b=Deinitialize the data path associated with host lane 8	RW RQD
	6	DataPathDeinit Host Lane 7	Data Path initialization control for host lane 7 0b=Initialize the data path associated with host lane 7 1b=Deinitialize the data path associated with host lane 7	
	5	DataPathDeinit Host Lane 6	Data Path initialization control for host lane 6 0b=Initialize the data path associated with host lane 6 1b=Deinitialize the data path associated with host lane 6	
	4	DataPathDeinit Host Lane 5	Data Path initialization control for host lane 5 0b=Initialize the data path associated with host lane 5 1b= Deinitialize the data path associated with host lane 5	

Byte	Bit	Name	Description	Type
	3	DataPathDeinit Host Lane 4	Data Path initialization control for host lane 4 0b=Initialize the data path associated with host lane 4 1b=Deinitialize the data path associated with host lane 4	
	2	DataPathDeinit Host Lane 3	Data Path initialization control for host lane 3 0b=Initialize the data path associated with host lane 4 1b=Deinitialize the data path associated with host lane 3	
	1	DataPathDeinit Host Lane 2	Data Path initialization control for host lane 2 0b=Initialize the data path associated with host lane 2 1b=Deinitialize the data path associated with host lane 2	
	0	DataPathDeinit Host Lane 1	Data Path initialization control for host lane 1 0b=Initialize the data path associated with host lane 1 1b=Deinitialize the data path associated with host lane 1	

8.7.2 Lane-Specific Direct Effect Control Fields

The following fields are provided to control certain properties of individual lanes in the module, independent of the data path. In some cases, behaviors may be overridden by data path characteristics (e.g. Tx Disable in DataPathInit). These settings are not staged and have no relationship to Control Sets.

When a Tx output is disabled, it shall have negligible optical output power (Average power <-20dBm). When a Tx output is squelched and not disabled, either the OMA or the Average power (Pave) is reduced on the optical output (See Table 8-31 and Table 8-7). In cases where both output Disable and Squelch are applied to the same channel, output Disable shall take precedence. If both Disable Tx Squelch and Force Tx Squelch are set for one or more channels, the module shall squelch the channel.

Table 8-46 Lane-specific Control Fields (Page 10h)

Byte	Bits	Name	Description	Type
129	7	Tx8 Polarity Flip	0b=No polarity flip for lane 8 1b=Tx input polarity flip for lane 8	RW Opt.
	6	Tx7 Polarity Flip	0b=No polarity flip for lane 7 1b=Tx input polarity flip for lane 7	
	5	Tx6 Polarity Flip	0b=No polarity flip for lane 6 1b=Tx input polarity flip for lane 6	
	4	Tx5 Polarity Flip	0b=No polarity flip for lane 5 1b=Tx input polarity flip for lane 5	
	3	Tx4 Polarity Flip	0b=No polarity flip for lane 4 1b=Tx input polarity flip for lane 4	
	2	Tx3 Polarity Flip	0b=No polarity flip for lane 3 1b=Tx input polarity flip for lane 3	
	1	Tx2 Polarity Flip	0b=No polarity flip for lane 2 1b=Tx input polarity flip for lane 2	
	0	Tx1 Polarity Flip	0b=No polarity flip for lane 1 1b=Tx input polarity flip for lane 1	
130	7	Tx8 Disable	0b=Tx output enabled for media lane 8 1b=Tx output disabled for media lane 8	RW Opt.
	6	Tx7 Disable	0b=Tx output enabled for media lane 7 1b=Tx output disabled for media lane 7	
	5	Tx6 Disable	0b=Tx output enabled for media lane 6 1b=Tx output disabled for media lane 6	
	4	Tx5 Disable	0b=Tx output enabled for media lane 5 1b=Tx output disabled for media lane 5	
	3	Tx4 Disable	0b=Tx output enabled for media lane 4 1b=Tx output disabled for media lane 4	
	2	Tx3 Disable	0b=Tx output enabled for media lane 3	

Byte	Bits	Name	Description	Type
			1b=Tx output disabled for media lane 3	
	1	Tx2 Disable	0b=Tx output enabled for media lane 2 1b=Tx output disabled for media lane 2	
	0	Tx1 Disable	0b=Tx output enabled for media lane 1 1b=Tx output disabled for media lane 1	
131	7	Tx8 Squelch Disable	0b=Tx output squelch permitted for media lane 8 when associated host input LOS is detected 1b=Tx output squelch not permitted for media lane 8	RW Opt.
	6	Tx7 Squelch Disable	0b=Tx output squelch permitted for media lane 7 when associated host input LOS is detected 1b=Tx output squelch not permitted for media lane 7	
	5	Tx6 Squelch Disable	0b=Tx output squelch permitted for media lane 6 when associated host input LOS is detected 1b=Tx output squelch not permitted for media lane 6	
	4	Tx5 Squelch Disable	0b=Tx output squelch permitted for media lane 5 when associated host input LOS is detected 1b=Tx output squelch not permitted for media lane 5	
	3	Tx4 Squelch Disable	0b=Tx output squelch permitted for media lane 4 when associated host input LOS is detected 1b=Tx output squelch not permitted for media lane 4	
	2	Tx3 Squelch Disable	0b=Tx output squelch permitted for media lane 3 when associated host input LOS is detected 1b=Tx output squelch not permitted for media lane 3	
	1	Tx2 Squelch Disable	0b=Tx output squelch permitted for media lane 2 when associated host input LOS is detected 1b=Tx output squelch not permitted for media lane 2	
	0	Tx1 Squelch Disable	0b=Tx output squelch permitted for media lane 1 when associated host input LOS is detected 1b=Tx output squelch not permitted for media lane 1	
132	7	Tx8 Force Squelch	0b=No impact on Tx behavior for media lane 8 1b=Tx output squelched for media lane 8	RW Opt.
	6	Tx7 Force Squelch	0b=No impact on Tx behavior for media lane 7 1b=Tx output squelched for media lane 7	
	5	Tx6 Force Squelch	0b=No impact on Tx behavior for media lane 6 1b=Tx output squelched for media lane 6	
	4	Tx5 Force Squelch	0b=No impact on Tx behavior for media lane 5 1b=Tx output squelched for media lane 5	
	3	Tx4 Force Squelch	0b=No impact on Tx behavior for media lane 4 1b=Tx output squelched for media lane 4	
	2	Tx3 Force Squelch	0b=No impact on Tx behavior for media lane 3 1b=Tx output squelched for media lane 3	
	1	Tx2 Force Squelch	0b=No impact on Tx behavior for media lane 2 1b=Tx output squelched for media lane 2	
	0	Tx1 Force Squelch	0b=No impact on Tx behavior for media lane 1 1b=Tx output squelched for media lane 1	
133	7:0	Reserved		RO
134	7	Tx8 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 8 1b=Tx input eq adaptation frozen at last value for lane 8	RW Opt.
	6	Tx7 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 7 1b=Tx input eq adaptation frozen at last value for lane 7	
	5	Tx6 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 6 1b=Tx input eq adaptation frozen at last value for lane 6	

Byte	Bits	Name	Description	Type
	4	Tx5 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 5 1b=Tx input eq adaptation frozen at last value for lane 5	
	3	Tx4 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 4 1b=Tx input eq adaptation frozen at last value for lane 4	
	2	Tx3 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 3 1b=Tx input eq adaptation frozen at last value for lane 3	
	1	Tx2 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 2 1b=Tx input eq adaptation frozen at last value for lane 2	
	0	Tx1 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 1 1b=Tx input eq adaptation frozen at last value for lane 1	
135	7-6	Tx4 Input Eq Adaptation Store	Tx Input Eq Adaptation Store location 00b=reserved 01b=store location 1 10b=store location 2 11b=reserved See section 6.2.4.4	WO Opt.
	5-4	Tx3 Input Eq Adaptation Store		
	3-2	Tx2 Input Eq Adaptation Store		
	1-0	Tx1 Input Eq Adaptation Store		
136	7-6	Tx8 Input Eq Adaptation Store	Tx Input Eq Adaptation Store location 00b=reserved 01b=store location 1 10b=store location 2 11b=reserved See section 6.2.4.4	WO Opt.
	5-4	Tx7 Input Eq Adaptation Store		
	3-2	Tx6 Input Eq Adaptation Store		
	1-0	Tx5 Input Eq Adaptation Store		
137	7	Rx8 Polarity Flip	0b=No polarity flip for lane 8 1b=Rx output polarity flip for lane 8	RW Opt.
	6	Rx7 Polarity Flip	0b=No polarity flip for lane 7 1b=Rx output polarity flip for lane 7	
	5	Rx6 Polarity Flip	0b=No polarity flip for lane 6 1b=Rx output polarity flip for lane 6	
	4	Rx5 Polarity Flip	0b=No polarity flip for lane 5 1b=Rx output polarity flip for lane 5	
	3	Rx4 Polarity Flip	0b=No polarity flip for lane 4 1b=Rx output polarity flip for lane 4	
	2	Rx3 Polarity Flip	0b=No polarity flip for lane 3 1b=Rx output polarity flip for lane 3	
	1	Rx2 Polarity Flip	0b=No polarity flip for lane 2 1b=Rx output polarity flip for lane 2	
	0	Rx1 Polarity Flip	0b=No polarity flip for lane 1 1b=Rx output polarity flip for lane 1	
138	7	Rx8 Output Disable	0b=Rx output enabled for lane 8 1b=Rx output disabled for lane 8	RW Opt.
	6	Rx7 Output Disable	0b=Rx output enabled for lane 7 1b=Rx output disabled for lane 7	
	5	Rx6 Output Disable	0b=Rx output enabled for lane 6 1b=Rx output disabled for lane 6	
	4	Rx5 Output Disable	0b=Rx output enabled for lane 5 1b=Rx output disabled for lane 5	
	3	Rx4 Output Disable	0b=Rx output enabled for lane 4 1b=Rx output disabled for lane 4	
	2	Rx3 Output Disable	0b=Rx output enabled for lane 3 1b=Rx output disabled for lane 3	
	1	Rx2 Output Disable	0b=Rx output enabled for lane 2 1b=Rx output disabled for lane 2	
	0	Rx1 Output Disable	0b=Rx output enabled for lane 1	

Byte	Bits	Name	Description	Type
			1b=Rx output disabled for lane 1	
139	7	Rx8 Squelch Disable	0b=Rx output squelch permitted for lane 8 1b=Rx output squelch not permitted for lane 8	RW Opt.
	6	Rx7 Squelch Disable	0b=Rx output squelch permitted for lane 7 1b=Rx output squelch not permitted for lane 7	
	5	Rx6 Squelch Disable	0b=Rx output squelch permitted for lane 6 1b=Rx output squelch not permitted for lane 6	
	4	Rx5 Squelch Disable	0b=Rx output squelch permitted for lane 5 1b=Rx output squelch not permitted for lane 5	
	3	Rx4 Squelch Disable	0b=Rx output squelch permitted for lane 4 1b=Rx output squelch not permitted for lane 4	
	2	Rx3 Squelch Disable	0b=Rx output squelch permitted for lane 3 1b=Rx output squelch not permitted for lane 3	
	1	Rx2 Squelch Disable	0b=Rx output squelch permitted for lane 2 1b=Rx output squelch not permitted for lane 2	
	0	Rx1 Squelch Disable	0b=Rx output squelch permitted for lane 1 1b=Rx output squelch not permitted for lane 1	
140-142	All	Reserved		RO

8.7.3 Staged Control Set 0

Staged Control Set 0 is required for all modules. Refer to section 6.2.3 for background on Control Set methodology.

8.7.3.1 Apply Controls

The host should write the Apply_DataPathInit and Apply_Immediate bytes with one-byte writes. Both bytes are write only. A read of these registers shall return 0.

Table 8-47 Staged Control Set 0, Apply Controls (Page 10h)

Byte	Bits	Name	Description	Type
143	7	Staged Set 0 Lane 8 Apply_DataPathInit	1b=Apply Staged Control Set 0 lane 8 settings using DataPathInit	WO RQD
	6	Staged Set 0 Lane 7 Apply_DataPathInit	1b=Apply Staged Control Set 0 lane 7 settings using DataPathInit	
	5	Staged Set 0 Lane 6 Apply_DataPathInit	1b=Apply Staged Control Set 0 lane 6 settings using DataPathInit	
	4	Staged Set 0 Lane 5 Apply_DataPathInit	1b=Apply Staged Control Set 0 lane 5 settings using DataPathInit	
	3	Staged Set 0 Lane 4 Apply_DataPathInit	1b=Apply Staged Control Set 0 lane 4 settings using DataPathInit	
	2	Staged Set 0 Lane 3 Apply_DataPathInit	1b=Apply Staged Control Set 0 lane 3 settings using DataPathInit	
	1	Staged Set 0 Lane 2 Apply_DataPathInit	1b=Apply Staged Control Set 0 lane 2 settings using DataPathInit	
	0	Staged Set 0 Lane 1 Apply_DataPathInit	1b=Apply Staged Control Set 0 lane 1 settings using DataPathInit	
144	7	Staged Set 0 Lane 8 Apply_Immediate	1b=Apply Staged Control Set 0 lane 8 settings with no Data Path State transitions	WO RQD
	6	Staged Set 0 Lane 7 Apply_Immediate	1b=Apply Staged Control Set 0 lane 7 settings with no Data Path State transitions	
	5	Staged Set 0 Lane 6 Apply_Immediate	1b=Apply Staged Control Set 0 lane 6 settings with no Data Path State transitions	
	4	Staged Set 0 Lane 5 Apply_Immediate	1b=Apply Staged Control Set 0 lane 5 settings with no Data Path State transitions	
	3	Staged Set 0 Lane 4 Apply_Immediate	1b=Apply Staged Control Set 0 lane 4 settings with no Data Path State transitions	
	2	Staged Set 0 Lane 3 Apply_Immediate	1b=Apply Staged Control Set 0 lane 3 settings with no Data Path State transitions	
	1	Staged Set 0 Lane 2 Apply_Immediate	1b=Apply Staged Control Set 0 lane 2 settings with no Data Path State transitions	
	0	Staged Set 0 Lane 1 Apply_Immediate	1b=Apply Staged Control Set 0 lane 1 settings with no Data Path State transitions	

8.7.3.2 Application Select Controls

The following fields allow the host to select one or more of the Applications supported and advertised by the module in Table 8-13 and Table 8-39. A set of fields is provided for each lane, however Applications that span multiple lanes shall have the same ApSel code and Data Path code for all lanes in the data path. Changes to these fields are not applied until the corresponding lane bits in Apply_DataPathInit or Apply_Immediate are set.

The ApSel Codes shall be one of the module-advertised ApSel Codes from Table 8-13 or Table 8-39, or a value of 0000b to indicate that the applicable lane is not part of any data path. The Data Path code identifies the first lane in the data path. For example, a data path including lane 1 would be coded 000b and a data path where lane 5 is the lower lane number would be coded 100b. Explicit Control (bit 0 in bytes 145-152) allows the host to specify

signal integrity settings rather than use the Application defined settings. These settings may be specified using Table 8-49 and Table 8-50.

Table 8-48 Staged Control Set 0, Application Select Controls (Page 10h)

Byte	Bits	Name	Description	Type
145	7-4	Staged Set 0 Lane 1 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 1	RW RQD
	3-1	Staged Set 0 Lane 1 Data Path ID	First lane of the data path containing lane 1 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 0 Lane 1 Explicit Control	0b=Use Application-defined settings for lane 1 1b=use Staged Set 0 control values for lane 1	
146	7-4	Staged Set 0 Lane 2 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 2	RW RQD
	3-1	Staged Set 0 Lane 2 Data Path ID	First lane of the data path containing lane 2 000b=Lane 1, 001b=Lane 2	
	0	Staged Set 0 Lane 2 Explicit Control	0b=Use Application-defined settings for lane 2 1b=use Staged Set 0 control values for lane 2	
147	7-4	Staged Set 0 Lane 3 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 3	RW RQD
	3-1	Staged Set 0 Lane 3 Data Path ID	First lane of the data path containing lane 3 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 0 Lane 3 Explicit Control	0b=Use Application-defined settings for lane 3 1b=use Staged Set 0 control values for lane 3	
148	7-4	Staged Set 0 Lane 4 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 4	RW RQD
	3-1	Staged Set 0 Lane 4 Data Path ID	First lane of the data path containing lane 4 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 0 Lane 4 Explicit Control	0b=Use Application-defined settings for lane 4 1b=use Staged Set 0 control values for lane 4	
149	7-4	Staged Set 0 Lane 5 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 5	RW RQD
	3-1	Staged Set 0 Lane 5 Data Path ID	First lane of the data path containing lane 5 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 0 Lane 5 Explicit Control	0b=Use Application-defined settings for lane 5 1b=use Staged Set 0 control values for lane 5	
150	7-4	Staged Set 0 Lane 6 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 6	RW RQD
	3-1	Staged Set 0 Lane 6 Data Path ID	First lane of the data path containing lane 6 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 0 Lane 6 Explicit Control	0b=Use Application-defined settings for lane 6 1b=use Staged Set 0 control values for lane 6	
151	7-4	Staged Set 0 Lane 7 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 7	RW RQD
	3-1	Staged Set 0 Lane 7 Data Path ID	First lane of the data path containing lane 7 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 0 Lane 7 Explicit Control	0b=Use Application-defined settings for lane 7 1b=use Staged Set 0 control values for lane 7	
152	7-4	Staged Set 0 Lane 8 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 8	RW RQD
	3-1	Staged Set 0 Lane 8 Data Path ID	First lane of the data path containing lane 8 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 0 Lane 8 Explicit Control	0b=Use Application default settings for lane 8 1b=use Staged Set 0 control values for lane 8	

8.7.3.3 Tx and Rx Signal Integrity Controls

The following fields allow the host to specify the signal integrity settings for a lane rather than use the defaults associated with the selected Application Code. See section 6.2.3 for the dependency of these fields on the value of the Explicit Control bit. Changes to these fields are not applied until the corresponding lane bits in Apply_DataPathInit or Apply_Immediate are set. See section 6.2.4 for definitions of valid signal integrity control settings.

Table 8-49 Staged Control Set 0, Tx Controls (Page 10h)

Byte	Bits	Name	Description	Type
153	7	Staged Set 0 Tx8 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	RW Req
	6	Staged Set 0 Tx7 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	5	Staged Set 0 Tx6 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	4	Staged Set 0 Tx5 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	3	Staged Set 0 Tx4 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	2	Staged Set 0 Tx3 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	1	Staged Set 0 Tx2 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	0	Staged Set 0 Tx1 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
154	7-6	Staged Set 0 Tx4 Adaptive Input Eq Recall	Recall stored Tx Eq adaptation value, 00b=do not Recall 01b=store location 1 10b=store location 2 11b=reserved See section 6.2.4.4 for Store/Recall methodology	RW Req
	5-4	Staged Set 0 Tx3 Adaptive Input Eq Recall		
	3-2	Staged Set 0 Tx2 Adaptive Input Eq Recall		
	1-0	Staged Set 0 Tx1 Adaptive Input Eq Recall		
155	7-6	Staged Set 0 Tx8 Adaptive Input Eq Recall	Recall stored Tx Eq adaptation value, 00b=do not Recall 01b=store location 1 10b=store location 2 11b=reserved See section 6.2.4.4 for Store/Recall methodology	RW Req
	5-4	Staged Set 0 Tx7 Adaptive Input Eq Recall		
	3-2	Staged Set 0 Tx6 Adaptive Input Eq Recall		
	1-0	Staged Set 0 Tx5 Adaptive Input Eq Recall		
156	7-4	Staged Set 0 Tx2 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	RW Req
	3-0	Staged Set 0 Tx1 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	
157	7-4	Staged Set 0 Tx4 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	RW Req
	3-0	Staged Set 0 Tx3 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	
158	7-4	Staged Set 0 Tx6 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	RW Req
	3-0	Staged Set 0 Tx5 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	
159	7-4	Staged Set 0 Tx8 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	RW Req
	3-0	Staged Set 0 Tx7 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	
160	7	Staged Set 0 Tx8 CDR control	1b=CDR enabled, 0b=CDR bypassed	RW Req
	6	Staged Set 0 Tx7 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	5	Staged Set 0 Tx6 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	4	Staged Set 0 Tx5 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	3	Staged Set 0 Tx4 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	2	Staged Set 0 Tx3 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	1	Staged Set 0 Tx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	0	Staged Set 0 Tx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	

Table 8-50 Staged Control Set 0, Rx Controls (Page 10h)

Byte	Bits	Name	Description	Type
161	7	Staged Set 0 Rx8 CDR control	1b=CDR enabled, 0b=CDR bypassed	RW Opt.
	6	Staged Set 0 Rx7 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	5	Staged Set 0 Rx6 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	4	Staged Set 0 Rx5 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	3	Staged Set 0 Rx4 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	2	Staged Set 0 Rx3 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	1	Staged Set 0 Rx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	0	Staged Set 0 Rx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	
162	7-4	Staged Set 0 Rx2 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	RW Opt.
	3-0	Staged Set 0 Rx1 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	
163	7-4	Staged Set 0 Rx4 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	RW Opt.
	3-0	Staged Set 0 Rx3 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	
164	7-4	Staged Set 0 Rx6 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	RW Opt.
	3-0	Staged Set 0 Rx5 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	
165	7-4	Staged Set 0 Rx8 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	RW Opt.
	3-0	Staged Set 0 Rx7 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	
166	7-4	Staged Set 0 Rx2 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	RW Opt.
	3-0	Staged Set 0 Rx1 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	
167	7-4	Staged Set 0 Rx4 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	RW Opt.
	3-0	Staged Set 0 Rx3 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	
168	7-4	Staged Set 0 Rx6 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	RW Opt.
	3-0	Staged Set 0 Rx5 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	
169	7-4	Staged Set 0 Rx8 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	RW Opt.
	3-0	Staged Set 0 Rx7 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	
170	7-4	Staged Set 0 Rx2 Output Amplitude control	Rx output amplitude[2]	RW Opt.
	3-0	Staged Set 0 Rx1 Output Amplitude control	Rx output amplitude[2]	
171	7-4	Staged Set 0 Rx4 Output Amplitude control	Rx output amplitude[2]	RW Opt.
	3-0	Staged Set 0 Rx3 Output Amplitude control	Rx output amplitude[2]	
172	7-4	Staged Set 0 Rx6 Output Amplitude control	Rx output amplitude[2]	RW Opt.
	3-0	Staged Set 0 Rx5 Output Amplitude control	Rx output amplitude[2]	
173	7-4	Staged Set 0 Rx8 Output Amplitude control	Rx output amplitude[2]	RW Opt.
	3-0	Staged Set 0 Rx7 Output Amplitude control	Rx output amplitude[2]	
174-177	All	Reserved		RO

Note 1: See Table 6-5
Note 2: See Table 6-6

8.7.4 Staged Control Set 1

Staged Control Set 1 is MSA optional for all modules but may be needed for some Applications where speed negotiation is performed. The module advertises support for Staged Control Set 1 in Table 8-28. Refer to section 6.2.3 for background on Control Set methodology.

8.7.4.1 Apply Controls

The host should write the Apply_DataPathInit and Apply_Immediate bytes with one-byte writes. Both bytes are write only. A read of these registers shall return 0.

Table 8-51 Staged Control Set 1, Apply Controls (Page 10h)

Byte	Bits	Name	Description	Type
178	7	Staged Set 1 Lane 8 Apply_DataPathInit	1b=Apply Staged Control Set 1 lane 8 settings using DataPathInit	WO Opt.
	6	Staged Set 1 Lane 7 Apply_DataPathInit	1b=Apply Staged Control Set 1 lane 7 settings using DataPathInit	
	5	Staged Set 1 Lane 6 Apply_DataPathInit	1b=Apply Staged Control Set 1 lane 6 settings using DataPathInit	
	4	Staged Set 1 Lane 5 Apply_DataPathInit	1b=Apply Staged Control Set 1 lane 5 settings using DataPathInit	
	3	Staged Set 1 Lane 4 Apply_DataPathInit	1b=Apply Staged Control Set 1 lane 4 settings using DataPathInit	
	2	Staged Set 1 Lane 3 Apply_DataPathInit	1b=Apply Staged Control Set 1 lane 3 settings using DataPathInit	
	1	Staged Set 1 Lane 2 Apply_DataPathInit	1b=Apply Staged Control Set 1 lane 2 settings using DataPathInit	
	0	Staged Set 1 Lane 1 Apply_DataPathInit	1b=Apply Staged Control Set 1 lane 1 settings using DataPathInit	
179	7	Staged Set 1 Lane 8 Apply_Immediate	1b=Apply Staged Control Set 1 lane 8 settings with no Data Path State transitions	WO Opt.
	6	Staged Set 1 Lane 7 Apply_Immediate	1b=Apply Staged Control Set 1 lane 7 settings with no Data Path State transitions	
	5	Staged Set 1 Ln6 Apply_Immediate	1b=Apply Staged Control Set 1 lane 6 settings with no Data Path State transitions	
	4	Staged Set 1 Lane 5 Apply_Immediate	1b=Apply Staged Control Set 1 lane 5 settings with no Data Path State transitions	
	3	Staged Set 1 Lane 4 Apply_Immediate	1b=Apply Staged Control Set 1 lane 4 settings with no Data Path State transitions	
	2	Staged Set 1 Lane 3 Apply_Immediate	1b=Apply Staged Control Set 1 lane 3 settings with no Data Path State transitions	
	1	Staged Set 1 Lane 2 Apply_Immediate	1b=Apply Staged Control Set 1 lane 2 settings with no Data Path State transitions	
	0	Staged Set 1 Lane 1 Apply_Immediate	1b=Apply Staged Control Set 1 lane 1 settings with no Data Path State transitions	

8.7.4.2 Application Select Controls

The following fields allow the host to select one or more of the Applications supported and advertised by the module in Table 8-13 and Table 8-38. A set of fields is provided for each lane, however Applications that span multiple lanes shall have the same Application code and Data Path code for all lanes in the data path. Changes to these fields are not applied until the corresponding lane bits in Apply_DataPathInit or Apply_Immediate are set.

The ApSel Codes shall be one of the module-advertised ApSel Codes from Table 8-13 or Table 8-39, or a value of 0000b to indicate that the applicable lane is not part of any data path. The Data Path code identifies the first lane in the data path. For example, a data path including lane 1 would be coded 000b and a data path where lane 5 is the lower lane number would be coded 100b. Explicit Control (bit 0 in bytes 180-187) allows the host to specify signal integrity settings rather than use the Application-defined settings. These settings may be specified using Table 8-53 and Table 8-54.

Table 8-52 Staged Control Set 1, Application Select Controls (Page 10h)

Byte	Bits	Name	Description	Type
180	7-4	Staged Set 1 Lane 1 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 1	RW Opt.
	3-1	Staged Set 1 Lane 1 Data Path ID	First lane in the data path containing lane 1 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 1 Lane 1 Explicit Control	0b=Use Application-defined settings for lane 1 1b=use Staged Set 1 control values for lane 1	
181	7-4	Staged Set 1 Lane 2 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 2	RW Opt.
	3-1	Staged Set 1 Lane 2 Data Path ID	First lane in the data path containing lane 2 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 1 Lane 2 Explicit Control	0b=Use Application-defined settings for lane 2 1b=use Staged Set 1 control values for lane 2	
182	7-4	Staged Set 1 Lane 3 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 3	RW Opt.
	3-1	Staged Set 1 Lane 3 Data Path ID	First lane in the data path containing lane 3 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 1 Lane 3 Explicit Control	0b=Use Application-defined settings for lane 3 1b=use Staged Set 1 control values for lane 3	
183	7-4	Staged Set 1 Lane 4 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 4	RW Opt.
	3-1	Staged Set 1 Lane 4 Data Path ID	First lane in the data path containing lane 4 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 1 Lane 4 Explicit Control	0b=Use Application-defined settings for lane 4 1b=use Staged Set 1 control values for lane 4	
184	7-4	Staged Set 1 Lane 5 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 5	RW Opt.
	3-1	Staged Set 1 Lane 5 Data Path ID	First lane in the data path containing lane 5 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 1 Lane 5 Explicit Control	0b=Use Application-defined settings for lane 5 1b=use Staged Set 1 control values for lane 5	
185	7-4	Staged Set 1 Lane 6 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 6	RW Opt.
	3-1	Staged Set 1 Lane 6 Data Path ID	First lane in the data path containing lane 6 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 1 Lane 6 Explicit Control	0b=Use Application-defined settings for lane 6 1b=use Staged Set 1 control values for lane 6	
186	7-4	Staged Set 1 Lane 7 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 7	RW Opt.
	3-1	Staged Set 1 Lane 7 Data Path ID	First lane in the data path containing lane 7 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 1 Lane 7 Explicit Control	0b=Use Application-defined settings for lane 7 1b=use Staged Set 1 control values for lane 7	
187	7-4	Staged Set 1 Lane 8 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 8	RW Opt.
	3-1	Staged Set 1 Lane 8 Data Path ID	First lane in the data path containing lane 8 000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 1 Lane 8 Explicit Control	0b=Use Application-defined settings for lane 8 1b=use Staged Set 1 control values for lane 8	

8.7.4.3 Tx and Rx Signal Integrity Controls

The following fields allow the host to specify the signal integrity settings for a lane rather than use the defaults associated with the selected ApSel Code. See section 6.2.3 for the dependency of these fields on the value of the

Explicit Control bit. Changes to these fields are not applied until the corresponding lane bits in Apply_DataPathInit or Apply_Immediate are set. See section 6.2.4 for definitions of valid signal integrity control settings.

Table 8-53 Staged Control Set 1, Tx Controls (Page 10h)

Byte	Bits	Name	Description	Type
188	7	Staged Set 1 Tx8 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	RW Opt.
	6	Staged Set 1 Tx7 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	5	Staged Set 1 Tx6 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	4	Staged Set 1 Tx5 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	3	Staged Set 1 Tx4 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	2	Staged Set 1 Tx3 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	1	Staged Set 1 Tx2 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
	0	Staged Set 1 Tx1 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	
189	7-6	Staged Set 1 Tx4 Adaptive Input Eq Recall	Recall stored Tx Eq adaptation value, 00b=do not recall 01b=store location 1 10b=store location 2 11b=reserved See section 6.2.4.4 for Store/Recall methodology	RW Opt.
	5-4	Staged Set 1 Tx3 Adaptive Input Eq Recall		
	3-2	Staged Set 1 Tx2 Adaptive Input Eq Recall		
	1-0	Staged Set 1 Tx1 Adaptive Input Eq Recall		
190	7-6	Staged Set 1 Tx8 Adaptive Input Eq Recall	Recall stored Tx Eq adaptation value, 00b=do not recall 01b=store location 1 10b=store location 2 11b=reserved See section 6.2.4.4 for Store/Recall methodology	RW Opt.
	5-4	Staged Set 1 Tx7 Adaptive Input Eq Recall		
	3-2	Staged Set 1 Tx6 Adaptive Input Eq Recall		
	1-0	Staged Set 1 Tx5 Adaptive Input Eq Recall		
191	7-4	Staged Set 1 Tx2 Input Eq control	Manual fixed Tx input eq control[1]	RW Opt.
	3-0	Staged Set 1 Tx1 Input Eq control	Manual fixed Tx input eq control[1]	
192	7-4	Staged Set 1 Tx4 Input Eq control	Manual fixed Tx input eq control[1]	RW Opt.
	3-0	Staged Set 1 Tx3 Input Eq control	Manual fixed Tx input eq control[1]	
193	7-4	Staged Set 1 Tx6 Input Eq control	Manual fixed Tx input eq control[1]	RW Opt.
	3-0	Staged Set 1 Tx5 Input Eq control	Manual fixed Tx input eq control[1]	
194	7-4	Staged Set 1 Tx8 Input Eq control	Manual fixed Tx input eq control[1]	RW Opt.
	3-0	Staged Set 1 Tx7 Input Eq control	Manual fixed Tx input eq control[1]	
195	7	Staged Set 1 Tx8 CDR control	1b=CDR enabled, 0b=CDR bypassed	RW Opt.
	6	Staged Set 1 Tx7 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	5	Staged Set 1 Tx6 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	4	Staged Set 1 Tx5 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	3	Staged Set 1 Tx4 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	2	Staged Set 1 Tx3 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	1	Staged Set 1 Tx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	0	Staged Set 1 Tx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	

Note 1: See Table 6-4

Table 8-54 Staged Control Set 1, Rx Controls (Page 10h)

Byte	Bits	Name	Description	Type
196	7	Staged Set 1 Rx8 CDR control	1b=CDR enabled, 0b=CDR bypassed	RW Opt.
	6	Staged Set 1 Rx7 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	5	Staged Set 1 Rx6 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	4	Staged Set 1 Rx5 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	3	Staged Set 1 Rx4 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	2	Staged Set 1 Rx3 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	1	Staged Set 1 Rx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	0	Staged Set 1 Rx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	
197	7-4	Staged Set 1 Rx2 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	RW Opt.
	3-0	Staged Set 1 Rx1 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	
198	7-4	Staged Set 1 Rx4 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	RW Opt.
	3-0	Staged Set 1 Rx3 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	
199	7-4	Staged Set 1 Rx6 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	RW Opt.
	3-0	Staged Set 1 Rx5 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	
200	7-4	Staged Set 1 Rx8 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	RW Opt.
	3-0	Staged Set 1 Rx7 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	
201	7-4	Staged Set 1 Rx2 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	RW Opt.
	3-0	Staged Set 1 Rx1 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	
202	7-4	Staged Set 1 Rx4 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	RW Opt.
	3-0	Staged Set 1 Rx3 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	
203	7-4	Staged Set 1 Rx6 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	RW Opt.
	3-0	Staged Set 1 Rx5 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	
204	7-4	Staged Set 1 Rx8 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	RW Opt.
	3-0	Staged Set 1 Rx7 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	
205	7-4	Staged Set 1 Rx2 Output Amplitude control	Rx output amplitude encoding[2]	RW Opt.
	3-0	Staged Set 1 Rx1 Output Amplitude control	Rx output amplitude encoding[2]	
206	7-4	Staged Set 1 Rx4 Output Amplitude control	Rx output amplitude encoding[2]	RW Opt.
	3-0	Staged Set 1 Rx3 Output Amplitude control	Rx output amplitude encoding[2]	
207	7-4	Staged Set 1 Rx6 Output Amplitude control	Rx output amplitude encoding[2]	RW Opt.
	3-0	Staged Set 1 Rx5 Output Amplitude control	Rx output amplitude encoding[2]	
208	7-4	Staged Set 1 Rx8 Output Amplitude control	Rx output amplitude encoding[2]	RW Opt.
	3-0	Staged Set 1 Rx7 Output Amplitude control	Rx output amplitude encoding[2]	
209-212	All	Reserved		RO

Note 1: See Table 6-5
Note 2: See Table 6-6

8.7.5 Lane-Specific Flag Masks

The host may control which flags result in a hardware interrupt by setting masking bits in Table 8-55. For example, the mask bits may be used to prevent an interrupt request from remaining active while the host performs actions to acknowledge and handle the interrupt condition. A mask bit is allocated for each flag bit.

A value of 1 in a masking bit prevents the assertion of the hardware interrupt signal, if one exists, by the corresponding latched flag bit. Masking bits are volatile: at exit from MgmtInit (see section 6.3.1.6), all mask bits shall be clear.

Table 8-55 Lane-Specific Flag Masks (Page 10h)

Byte	Bits	Name	Description	Type
213	7	M- Data Path State Changed flag mask, host lane 8	Masking bit for Data Path State Changed flag, host lane 8	RW RQD
	6	M-Data Path State Changed flag mask, host lane 7	Masking bit for Data Path State Changed flag, host lane 7	
	5	M-Data Path State Changed flag mask, host lane 6	Masking bit for Data Path State Changed flag, host lane 6	
	4	M-Data Path State Changed flag mask, host lane 5	Masking bit for Data Path State Changed flag, host lane 5	
	3	M-Data Path State Changed flag mask, host lane 4	Masking bit for Data Path State Changed flag, host lane 4	
	2	M-Data Path State Changed flag mask, host lane 3	Masking bit for Data Path State Changed flag, host lane 3	
	1	M-Data Path State Changed flag mask, host lane 2	Masking bit for Data Path State Changed flag, host lane 2	
	0	M-Data Path State Changed flag mask, host lane 1	Masking bit for Data Path State Changed flag, host lane 1	
214	7	M-Tx8 Fault flag mask	Masking bit for Tx Fault flag, media lane 8	RW Opt.
	6	M-Tx7 Fault flag mask	Masking bit for Tx Fault flag, media lane 7	
	5	M-Tx6 Fault flag mask	Masking bit for Tx Fault flag, media lane 6	
	4	M-Tx5 Fault flag mask	Masking bit for Tx Fault flag, media lane 5	
	3	M-Tx4 Fault flag mask	Masking bit for Tx Fault flag, media lane 4	
	2	M-Tx3 Fault flag mask	Masking bit for Tx Fault flag, media lane 3	
	1	M-Tx2 Fault flag mask	Masking bit for Tx Fault flag, media lane 2	
	0	M-Tx1 Fault flag mask	Masking bit for Tx Fault flag, media lane 1	
215	7	M-Tx8 LOS flag mask	Masking bit for Tx LOS flag, lane 8	RW Opt.
	6	M-Tx7 LOS flag mask	Masking bit for Tx LOS flag, lane 7	
	5	M-Tx6 LOS flag mask	Masking bit for Tx LOS flag, lane 6	
	4	M-Tx5 LOS flag mask	Masking bit for Tx LOS flag, lane 5	
	3	M-Tx4 LOS flag mask	Masking bit for Tx LOS flag, lane 4	
	2	M-Tx3 LOS flag mask	Masking bit for Tx LOS flag, lane 3	
	1	M-Tx2 LOS flag mask	Masking bit for Tx LOS flag, lane 2	
	0	M-Tx1 LOS flag mask	Masking bit for Tx LOS flag, lane 1	
216	7	M-Tx8 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 8	RW Opt.
	6	M-Tx7 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 7	
	5	M-Tx6 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 6	
	4	M-Tx5 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 5	
	3	M-Tx4 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 4	
	2	M-Tx3 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 3	
	1	M-Tx2 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 2	
	0	M-Tx1 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 1	
217	7	M-Tx8 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 8	RW Opt.
	6	M-Tx7 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 7	
	5	M-Tx6 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 6	
	4	M-Tx5 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 5	
	3	M-Tx4 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 4	
	2	M-Tx3 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 3	
	1	M-Tx2 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 2	
	0	M-Tx1 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 1	
218	7	M-Tx8 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 8	RW Opt.
	6	M-Tx7 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 7	

Byte	Bits	Name	Description	Type
	5	M-Tx6 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 6	
	4	M-Tx5 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 5	
	3	M-Tx4 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 4	
	2	M-Tx3 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 3	
	1	M-Tx2 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 2	
	0	M-Tx1 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 1	
219	7	M-Tx8 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 8	RW Opt.
	6	M-Tx7 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 7	
	5	M-Tx6 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 6	
	4	M-Tx5 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 5	
	3	M-Tx4 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 4	
	2	M-Tx3 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 3	
	1	M-Tx2 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 2	
	0	M-Tx1 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 1	
220	7	M-Tx8 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 8	RW Opt.
	6	M-Tx7 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 7	
	5	M-Tx6 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 6	
	4	M-Tx5 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 5	
	3	M-Tx4 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 4	
	2	M-Tx3 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 3	
	1	M-Tx2 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 2	
	0	M-Tx1 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 1	
221	7	M-Tx8 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 8	RW Opt.
	6	M-Tx7 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 7	
	5	M-Tx6 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 6	
	4	M-Tx5 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 5	
	3	M-Tx4 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 4	
	2	M-Tx3 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 3	
	1	M-Tx2 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 2	
	0	M-Tx1 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 1	
222	7	M-Tx8 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 8	RW Opt.
	6	M-Tx7 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 7	
	5	M-Tx6 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 6	
	4	M-Tx5 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 5	
	3	M-Tx4 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 4	
	2	M-Tx3 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 3	
	1	M-Tx2 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 2	

Byte	Bits	Name	Description	Type
	0	M-Tx1 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 1	
223	7	M-Tx8 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 8	RW Opt.
	6	M-Tx7 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 7	
	5	M-Tx6 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 6	
	4	M-Tx5 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 5	
	3	M-Tx4 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 4	
	2	M-Tx3 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 3	
	1	M-Tx2 Bias Low Alarm flag mask	Masking bit for Tx Bias Low Alarm, media lane 2	
	0	M-Tx1 Bias Low Alarm flag mask	Masking bit for Tx Bias Low Alarm, media lane 1	
224	7	M-Tx8 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 8	RW Opt.
	6	M-Tx7 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 7	
	5	M-Tx6 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 6	
	4	M-Tx5 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 5	
	3	M-Tx4 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 4	
	2	M-Tx3 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 3	
	1	M-Tx2 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 2	
	0	M-Tx1 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 1	
225	7	M-Tx8 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 8	RW Opt.
	6	M-Tx7 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 7	
	5	M-Tx6 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 6	
	4	M-Tx5 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 5	
	3	M-Tx4 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 4	
	2	M-Tx3 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 3	
	1	M-Tx2 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 2	
	0	M-Tx1 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 1	
226	7	M-Rx8 LOS flag mask	Masking bit for Rx LOS flag, media lane 8	RW Opt.
	6	M-Rx7 LOS flag mask	Masking bit for Rx LOS flag, media lane 7	
	5	M-Rx6 LOS flag mask	Masking bit for Rx LOS flag, media lane 6	
	4	M-Rx5 LOS flag mask	Masking bit for Rx LOS flag, media lane 5	
	3	M-Rx4 LOS flag mask	Masking bit for Rx LOS flag, media lane 4	
	2	M-Rx3 LOS flag mask	Masking bit for Rx LOS flag, media lane 3	
	1	M-Rx2 LOS flag mask	Masking bit for Rx LOS flag, media lane 2	
	0	M-Rx1 LOS flag mask	Masking bit for Rx LOS flag, media lane 1	
227	7	M-Rx8 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 8	RW Opt.
	6	M-Rx7 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 7	
	5	M-Rx6 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 6	
	4	M-Rx5 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 5	
	3	M-Rx4 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 4	
	2	M-Rx3 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 3	
	1	M-Rx2 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 2	
	0	M-Rx1 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 1	
228	7	M-Rx8 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 8	RW Opt.
	6	M-Rx7 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 7	
	5	M-Rx6 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 6	
	4	M-Rx5 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 5	
	3	M-Rx4 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 4	
	2	M-Rx3 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 3	
	1	M-Rx2 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 2	
	0	M-Rx1 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 1	
229	7	M-Rx8 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 8	RW Opt.
	6	M-Rx7 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 7	
	5	M-Rx6 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 6	

Byte	Bits	Name	Description	Type
	4	M-Rx5 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 5	
	3	M-Rx4 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 4	
	2	M-Rx3 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 3	
	1	M-Rx2 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 2	
	0	M-Rx1 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 1	
230	7	M-Rx8 Power High Warning flag mask	Masking bit for Rx input power High Warning, media lane 8	RW Opt.
	6	M-Rx7 Power High Warning flag mask	Masking bit for Rx input power High Warning, media lane 7	
	5	M-Rx6 Power High Warning flag mask	Masking bit for Rx input power High Warning, media lane 6	
	4	M-Rx5 Power High Warning flag mask	Masking bit for Rx input power High Warning, media lane 5	
	3	M-Rx4 Power High Warning flag mask	Masking bit for Rx input power High Warning, media lane 4	
	2	M-Rx3 Power High Warning flag mask	Masking bit for Rx input power High Warning, media lane 3	
	1	M-Rx2 Power High Warning flag mask	Masking bit for Rx input power High Warning, media lane 2	
	0	M-Rx1 Power High Warning flag mask	Masking bit for Rx input power High Warning, media lane 1	
231	7	M-Rx8 Power Low Warning flag mask	Masking bit for Rx input power Low Warning, media lane 8	RW Opt.
	6	M-Rx7 Power Low Warning flag mask	Masking bit for Rx input power Low Warning, media lane 7	
	5	M-Rx6 Power Low Warning flag mask	Masking bit for Rx input power Low Warning, media lane 6	
	4	M-Rx5 Power Low Warning flag mask	Masking bit for Rx input power Low Warning, media lane 5	
	3	M-Rx4 Power Low Warning flag mask	Masking bit for Rx input power Low Warning, media lane 4	
	2	M-Rx3 Power Low Warning flag mask	Masking bit for Rx input power Low Warning, media lane 3	
	1	M-Rx2 Power Low Warning flag mask	Masking bit for Rx input power Low Warning, media lane 2	
	0	M-Rx1 Power Low Warning flag mask	Masking bit for Rx input power Low Warning, media lane 1	

8.8 Page 11h (Lane Status)

The upper memory map page 11h is a banked page that contains lane dynamic status bytes. The presence of Page 11h is conditional on the state of bit 7 in Page 00h byte 2. All fields on Page 11h are read-only. Upper page 11h is subdivided into several areas as illustrated in the following table:

Table 8-56 Page 11h Overview

Byte	Size (bytes)	Name	Description
128-131	4	Data Path State indicators	
132-133	2	Reserved	
134-152	19	Lane-specific flags	
153	1	Reserved	
154-201	48	Lane-specific monitors	
202-205	4	Configuration Error Codes	Indicates validity of select Application codes
206-234	29	Active Control Set	
235-239	5	Reserved	
240-255	16	Host Electrical to Module Media Lane Mapping	Indicates the mapping of Host Electrical lanes to Module Media lanes

8.8.1 Data Path State Indicator

The following fields identify the Data Path State associated with each host lane in the module. Data Path States apply to the host and media interfaces, but are reported by host lane. For data paths with multiple lanes, all lanes shall report the same state. An indication of DataPathDeactivated means no data path is initialized on that lane. Table 8-58 defines the valid Data Path State encodings.

Table 8-57 Data Path State Indicator, per lane (Page 11h) (see Table 8-58)

Byte	Bit	Name	Description	Type
128	7-4	Data Path State host lane 2	Data path state encoding, as observed on host lane 2	RO
	3-0	Data Path State host lane 1	Data path state encoding, as observed on host lane 1	RQD
129	7-4	Data Path State host lane 4	Data path state encoding, as observed on host lane 4	RO
	3-0	Data Path State host lane 3	Data path state encoding, as observed on host lane 3	RQD
130	7-4	Data Path State host lane 6	Data path state encoding, as observed on host lane 6	RO
	3-0	Data Path State host lane 5	Data path state encoding, as observed on host lane 5	RQD
131	7-4	Data Path State host lane 8	Data path state encoding, as observed on host lane 8	RO
	3-0	Data Path State host lane 7	Data path state encoding, as observed on host lane 7	RQD

Table 8-58 Data Path State Indicator Encodings

Encoding	State
0h	Reserved
1h	DataPathDeactivated State
2h	DataPathInit State
3h	DataPathDeinit State
4h	DataPathActivated State
5h	DataPathTxTurnOn State
6h	DataPathTxTurnOff State
7h	DataPathInitialized State
8h-Fh	Reserved

8.8.2 Lane-Specific Flags

This section of the memory map contains lane-specific flags. These flags provide a mechanism for reporting lane-specific status changes, faults, operating failures and alarms and warnings for monitored attributes. Each lane-specific flag shall have an associated flag mask. Monitored attributes with associated alarm and/or warning thresholds shall implement associated alarm and warning flags and flag masks. For normal operation and default state, the bits in this field have the value of 0b. Once asserted, the bits remain set (latched) until cleared by a read operation that includes the affected bit or reset by the Reset signal. Note that a read of the flag summary shall not clear the underlying flag condition. If the corresponding mask bit is not set (see Table 8-55), Interrupt is also asserted at the onset of the condition and remains asserted until all asserted flags (both module-level and lane-specific) have been cleared by a host read. After being read and cleared, the bit shall be set again if the condition persists; this will cause Interrupt to be asserted again unless masked. The lane-specific flags are defined in Table 8-59, Table 8-60 and Table 8-61.

Table 8-59 Lane-Specific State Changed Flags (Page 11h)

Byte	Bit	Name	Description	Type
134	7	L-Data Path State Changed flag, host lane 8	Latched Data Path State Changed flag for host lane 8	RO/COR RQD
	6	L-Data Path State changed flag, host lane 7	Latched Data Path State Changed flag for host lane 7	
	5	L-Data Path State Changed flag, host lane 6	Latched Data Path State Changed flag for host lane 6	
	4	L-Data Path State Changed flag, host lane 5	Latched Data Path State Changed flag for host lane 5	
	3	L-Data Path State Changed flag, host lane 4	Latched Data Path State Changed flag for host lane 4	
	2	L-Data Path State Changed flag, host lane 3	Latched Data Path State Changed flag for host lane 3	
	1	L-Data Path State Changed flag, host lane 2	Latched Data Path State Changed flag for host lane 2	
	0	L-Data Path State Changed flag, host lane 1	Latched Data Path State Changed flag for host lane 1	

Table 8-60 Lane-Specific Tx Flags (Page 11h)

Byte	Bit	Name	Description	Type
135	7	L-Tx8 Fault flag	Latched Tx Fault flag, media lane 8	RO Opt.
	6	L-Tx7 Fault flag	Latched Tx Fault flag, media lane 7	
	5	L-Tx6 Fault flag	Latched Tx Fault flag, media lane 6	
	4	L-Tx5 Fault flag	Latched Tx Fault flag, media lane 5	
	3	L-Tx4 Fault flag	Latched Tx Fault flag, media lane 4	
	2	L-Tx3 Fault flag	Latched Tx Fault flag, media lane 3	
	1	L-Tx2 Fault flag	Latched Tx Fault flag, media lane 2	
	0	L-Tx1 Fault flag	Latched Tx Fault flag, media lane 1	
136	7	L-Tx8 LOS flag	Latched Tx LOS flag, lane 8	RO Opt.
	6	L-Tx7 LOS flag	Latched Tx LOS flag, lane 7	
	5	L-Tx6 LOS flag	Latched Tx LOS flag, lane 6	
	4	L-Tx5 LOS flag	Latched Tx LOS flag, lane 5	
	3	L-Tx4 LOS flag	Latched Tx LOS flag, lane 4	
	2	L-Tx3 LOS flag	Latched Tx LOS flag, lane 3	
	1	L-Tx2 LOS flag	Latched Tx LOS flag, lane 2	
	0	L-Tx1 LOS flag	Latched Tx LOS flag, lane 1	
137	7	L-Tx8 CDR LOL flag	Latched Tx CDR LOL flag, lane 8. Clear on Read	RO

Byte	Bit	Name	Description	Type
	6	L-Tx7 CDR LOL flag	Latched Tx CDR LOL flag, lane 7. Clear on Read	Opt.
	5	L-Tx6 CDR LOL flag	Latched Tx CDR LOL flag, lane 6. Clear on Read	
	4	L-Tx5 CDR LOL flag	Latched Tx CDR LOL flag, lane 5. Clear on Read	
	3	L-Tx4 CDR LOL flag	Latched Tx CDR LOL flag, lane 4. Clear on Read	
	2	L-Tx3 CDR LOL flag	Latched Tx CDR LOL flag, lane 3. Clear on Read	
	1	L-Tx2 CDR LOL flag	Latched Tx CDR LOL flag, lane 2. Clear on Read	
	0	L-Tx1 CDR LOL flag	Latched Tx CDR LOL flag, lane 1. Clear on Read	
138	7	L-Tx8 Adaptive Input Eq Fault Lane 8 flag	Latched Tx Adaptive Input Eq. Fault Lane 8. Clear on Read	RO Opt.
	6	L-Tx7 Adaptive Input Eq Fault Lane 7 flag	Latched Tx Adaptive Input Eq. Fault Lane 7. Clear on Read	
	5	L-Tx6 Adaptive Input Eq Fault Lane 6 flag	Latched Tx Adaptive Input Eq. Fault Lane 6. Clear on Read	
	4	L-Tx5 Adaptive Input Eq Fault Lane 5 flag	Latched Tx Adaptive Input Eq. Fault Lane 5. Clear on Read	
	3	L-Tx4 Adaptive Input Eq Fault Lane 4 flag	Latched Tx Adaptive Input Eq. Fault Lane 4. Clear on Read	
	2	L-Tx3 Adaptive Input Eq Fault Lane 3 flag	Latched Tx Adaptive Input Eq. Fault Lane 3. Clear on Read	
	1	L-Tx2 Adaptive Input Eq Fault Lane 2 flag	Latched Tx Adaptive Input Eq. Fault Lane 2. Clear on Read	
	0	L-Tx1 Adaptive Input Eq Fault Lane 1 flag	Latched Tx Adaptive Input Eq. Fault Lane 1. Clear on Read	
139	7	L-Tx8 Power High alarm	Tx output power High Alarm, media lane 8. Clear on Read	RO Opt.
	6	L-Tx7 Power High alarm	Tx output power High Alarm, media lane 7. Clear on Read	
	5	L-Tx6 Power High alarm	Tx output power High Alarm, media lane 6. Clear on Read	
	4	L-Tx5 Power High alarm	Tx output power High Alarm, media lane 5. Clear on Read	
	3	L-Tx4 Power High alarm	Tx output power High Alarm, media lane 4. Clear on Read	
	2	L-Tx3 Power High alarm	Tx output power High Alarm, media lane 3. Clear on Read	
	1	L-Tx2 Power High alarm	Tx output power High Alarm, media lane 2. Clear on Read	
	0	L-Tx1 Power High alarm	Tx output power High Alarm, media lane 1. Clear on Read	
140	7	L-Tx8 Power Low alarm	Tx output power Low alarm, media lane 8. Clear on Read	RO Opt.
	6	L-Tx7 Power Low alarm	Tx output power Low alarm, media lane 7. Clear on Read	
	5	L-Tx6 Power Low alarm	Tx output power Low alarm, media lane 6. Clear on Read	
	4	L-Tx5 Power Low alarm	Tx output power Low alarm, media lane 5. Clear on Read	
	3	L-Tx4 Power Low alarm	Tx output power Low alarm, media lane 4. Clear on Read	
	2	L-Tx3 Power Low alarm	Tx output power Low alarm, media lane 3. Clear on Read	
	1	L-Tx2 Power Low alarm	Tx output power Low alarm, media lane 2. Clear on Read	
	0	L-Tx1 Power Low alarm	Tx output power Low alarm, media lane 1. Clear on Read	
141	7	L-Tx8 Power High warning	Tx output power High warning, media lane 8. Clear on Read	RO Opt.
	6	L-Tx7 Power High warning	Tx output power High warning, media lane 7. Clear on Read	
	5	L-Tx6 Power High warning	Tx output power High warning, media lane 6. Clear on Read	
	4	L-Tx5 Power High warning	Tx output power High warning, media lane 5. Clear on Read	
	3	L-Tx4 Power High warning	Tx output power High warning, media lane 4. Clear on Read	
	2	L-Tx3 Power High warning	Tx output power High warning, media lane 3. Clear on Read	
	1	L-Tx2 Power High warning	Tx output power High warning, media lane 2. Clear on Read	
	0	L-Tx1 Power High warning	Tx output power High warning, media lane 1. Clear on Read	
142	7	L-Tx8 Power Low warning	Tx output power Low warning, media lane 8. Clear on Read	RO Opt.
	6	L-Tx7 Power Low warning	Tx output power Low warning, media lane 7. Clear on Read	
	5	L-Tx6 Power Low warning	Tx output power Low warning, media lane 6. Clear on Read	
	4	L-Tx5 Power Low warning	Tx output power Low warning, media lane 5. Clear on Read	

Byte	Bit	Name	Description	Type
	3	L-Tx4 Power Low warning	Tx output power Low warning, media lane 4. Clear on Read	
	2	L-Tx3 Power Low warning	Tx output power Low warning, media lane 3. Clear on Read	
	1	L-Tx2 Power Low warning	Tx output power Low warning, media lane 2. Clear on Read	
	0	L-Tx1 Power Low warning	Tx output power Low warning, media lane 1. Clear on Read	
143	7	L-Tx8 Bias High Alarm	Tx Bias High Alarm, media lane 8. Clear on Read	RO Opt.
	6	L-Tx7 Bias High Alarm	Tx Bias High Alarm, media lane 7. Clear on Read	
	5	L-Tx6 Bias High Alarm	Tx Bias High Alarm, media lane 6. Clear on Read	
	4	L-Tx5 Bias High Alarm	Tx Bias High Alarm, media lane 5. Clear on Read	
	3	L-Tx4 Bias High Alarm	Tx Bias High Alarm, media lane 4. Clear on Read	
	2	L-Tx3 Bias High Alarm	Tx Bias High Alarm, media lane 3. Clear on Read	
	1	L-Tx2 Bias High Alarm	Tx Bias High Alarm, media lane 2. Clear on Read	
	0	L-Tx1 Bias High Alarm	Tx Bias High Alarm, media lane 1. Clear on Read	
144	7	L-Tx8 Bias Low alarm	Tx Bias Low alarm, media lane 8. Clear on Read	RO Opt.
	6	L-Tx7 Bias Low alarm	Tx Bias Low alarm, media lane 7. Clear on Read	
	5	L-Tx6 Bias Low alarm	Tx Bias Low alarm, media lane 6. Clear on Read	
	4	L-Tx5 Bias Low alarm	Tx Bias Low alarm, media lane 5. Clear on Read	
	3	L-Tx4 Bias Low alarm	Tx Bias Low alarm, media lane 4. Clear on Read	
	2	L-Tx3 Bias Low alarm	Tx Bias Low alarm, media lane 3. Clear on Read	
	1	L-Tx2 Bias Low alarm	Tx Bias Low alarm, media lane 2. Clear on Read	
	0	L-Tx1 Bias Low alarm	Tx Bias Low alarm, media lane 1. Clear on Read	
145	7	L-Tx8 Bias High warning	Tx Bias High warning, media lane 8. Clear on Read	RO Opt.
	6	L-Tx7 Bias High warning	Tx Bias High warning, media lane 7. Clear on Read	
	5	L-Tx6 Bias High warning	Tx Bias High warning, media lane 6. Clear on Read	
	4	L-Tx5 Bias High warning	Tx Bias High warning, media lane 5. Clear on Read	
	3	L-Tx4 Bias High warning	Tx Bias High warning, media lane 4. Clear on Read	
	2	L-Tx3 Bias High warning	Tx Bias High warning, media lane 3. Clear on Read	
	1	L-Tx2 Bias High warning	Tx Bias High warning, media lane 2. Clear on Read	
	0	L-Tx1 Bias High warning	Tx Bias High warning, media lane 1. Clear on Read	
146	7	L-Tx8 Bias Low warning	Tx Bias Low warning, media lane 8. Clear on Read	RO Opt.
	6	L-Tx7 Bias Low warning	Tx Bias Low warning, media lane 7. Clear on Read	
	5	L-Tx6 Bias Low warning	Tx Bias Low warning, media lane 6. Clear on Read	
	4	L-Tx5 Bias Low warning	Tx Bias Low warning, media lane 5. Clear on Read	
	3	L-Tx4 Bias Low warning	Tx Bias Low warning, media lane 4. Clear on Read	
	2	L-Tx3 Bias Low warning	Tx Bias Low warning, media lane 3. Clear on Read	
	1	L-Tx2 Bias Low warning	Tx Bias Low warning, media lane 2. Clear on Read	
	0	L-Tx1 Bias Low warning	Tx Bias Low warning, media lane 1. Clear on Read	

Table 8-61 Rx Flags (Page 11h)

Byte	Bit	Name	Description	Type
147	7	L-Rx8 LOS	Latched Rx LOS flag, media lane 8. Clear on Read	RO Opt.
	6	L-Rx7 LOS	Latched Rx LOS flag, media lane 7. Clear on Read	
	5	L-Rx6 LOS	Latched Rx LOS flag, media lane 6. Clear on Read	
	4	L-Rx5 LOS	Latched Rx LOS flag, media lane 5. Clear on Read	
	3	L-Rx4 LOS	Latched Rx LOS flag, media lane 4. Clear on Read	
	2	L-Rx3 LOS	Latched Rx LOS flag, media lane 3. Clear on Read	
	1	L-Rx2 LOS	Latched Rx LOS flag, media lane 2. Clear on Read	
	0	L-Rx1 LOS	Latched Rx LOS flag, media lane 1. Clear on Read	
148	7	L-Rx8 CDR LOL	Latched Rx CDR LOL flag, media lane 8. Clear on Read	RO Opt.
	6	L-Rx7 CDR LOL	Latched Rx CDR LOL flag, media lane 7. Clear on Read	
	5	L-Rx6 CDR LOL	Latched Rx CDR LOL flag, media lane 6. Clear on Read	
	4	L-Rx5 CDR LOL	Latched Rx CDR LOL flag, media lane 5. Clear on Read	
	3	L-Rx4 CDR LOL	Latched Rx CDR LOL flag, media lane 4. Clear on Read	

Byte	Bit	Name	Description	Type
	2	L-Rx3 CDR LOL	Latched Rx CDR LOL flag, media lane 3. Clear on Read	
	1	L-Rx2 CDR LOL	Latched Rx CDR LOL flag, media lane 2. Clear on Read	
	0	L-Rx1 CDR LOL	Latched Rx CDR LOL flag, media lane 1. Clear on Read	
149	7	L-Rx8 Power High alarm	Rx input power High alarm, media lane 8. Clear on Read	RO Opt.
	6	L-Rx7 Power High alarm	Rx input power High alarm, media lane 7. Clear on Read	
	5	L-Rx6 Power High alarm	Rx input power High alarm, media lane 6. Clear on Read	
	4	L-Rx5 Power High alarm	Rx input power High alarm, media lane 5. Clear on Read	
	3	L-Rx4 Power High alarm	Rx input power High alarm, media lane 4. Clear on Read	
	2	L-Rx3 Power High alarm	Rx input power High alarm, media lane 3. Clear on Read	
	1	L-Rx2 Power High alarm	Rx input power High alarm, media lane 2. Clear on Read	
	0	L-Rx1 Power High alarm	Rx input power High alarm, media lane 1. Clear on Read	
150	7	L-Rx8 Power Low alarm	Rx input power Low alarm, media lane 8. Clear on Read	RO Opt.
	6	L-Rx7 Power Low alarm	Rx input power Low alarm, media lane 7. Clear on Read	
	5	L-Rx6 Power Low alarm	Rx input power Low alarm, media lane 6. Clear on Read	
	4	L-Rx5 Power Low alarm	Rx input power Low alarm, media lane 5. Clear on Read	
	3	L-Rx4 Power Low alarm	Rx input power Low alarm, media lane 4. Clear on Read	
	2	L-Rx3 Power Low alarm	Rx input power Low alarm, media lane 3. Clear on Read	
	1	L-Rx2 Power Low alarm	Rx input power Low alarm, media lane 2. Clear on Read	
	0	L-Rx1 Power Low alarm	Rx input power Low alarm, media lane 1. Clear on Read	
151	7	L-Rx8 Power High warning	Rx input power High warning, media lane 8. Clear on Read	RO Opt.
	6	L-Rx7 Power High warning	Rx input power High warning, media lane 7. Clear on Read	
	5	L-Rx6 Power High warning	Rx input power High warning, media lane 6. Clear on Read	
	4	L-Rx5 Power High warning	Rx input power High warning, media lane 5. Clear on Read	
	3	L-Rx4 Power High warning	Rx input power High warning, media lane 4. Clear on Read	
	2	L-Rx3 Power High warning	Rx input power High warning, media lane 3. Clear on Read	
	1	L-Rx2 Power High warning	Rx input power High warning, media lane 2. Clear on Read	
	0	L-Rx1 Power High warning	Rx input power High warning, media lane 1. Clear on Read	
152	7	L-Rx8 Power Low warning	Rx input power Low warning, media lane 8. Clear on Read	RO Opt.
	6	L-Rx7 Power Low warning	Rx input power Low warning, media lane 7. Clear on Read	
	5	L-Rx6 Power Low warning	Rx input power Low warning, media lane 6. Clear on Read	
	4	L-Rx5 Power Low warning	Rx input power Low warning, media lane 5. Clear on Read	
	3	L-Rx4 Power Low warning	Rx input power Low warning, media lane 4. Clear on Read	
	2	L-Rx3 Power Low warning	Rx input power Low warning, media lane 3. Clear on Read	
	1	L-Rx2 Power Low warning	Rx input power Low warning, media lane 2. Clear on Read	
	0	L-Rx1 Power Low warning	Rx input power Low warning, media lane 1. Clear on Read	

8.8.3 Lane-Specific Monitors

Real time lane monitoring may be performed for each transmit and receive lane and includes Tx output optical power, Rx input optical power, and Tx bias current. Alarm threshold values and warning threshold values have the same numerical value representation as the associated monitor values for which they specify threshold values.

Measured Tx bias current is represented as a 16-bit unsigned integer with the current defined as the full 16-bit value (0 to 65535) with LSB equal to 2 uA times the multiplier from page 01h byte 160. For a multiplier of 1, this yields a total measurement range of 0 to 131 mA. Accuracy is Vendor Specific but must be better than +/-10% of the manufacturer's nominal value over specified operating temperature and voltage.

Measured Rx input optical power is in mW and can represent either average received power or OMA depending the Rx Optical Power Measurement type in Table 8-30. The parameter is encoded as a 16-bit unsigned integer with the power defined as the full 16-bit value (0 to 65535) with LSB equal to 0.1 uW, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm). Absolute accuracy is dependent upon the exact optical wavelength. For the vendor specified wavelength, accuracy shall be better than +/-3 dB over specified

temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss (insertion loss or passive loss) per the appropriate standard. Absolute accuracy beyond this minimum required received input optical power range is Vendor Specific.

Measured Tx optical power is the average power represented in mW. The parameter is encoded as a 16-bit unsigned integer with the power defined as the full 16-bit value (0 to 65535) with LSB equal to 0.1 uW, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm). For the vendor specified wavelength, accuracy shall be better than +/-3 dB over specified temperature and voltage.

Table 8-62 Media Lane-Specific Monitors (Page 11h)

Byte	Bit	Name	Description	Type
153	7-0	Reserved		RO
154	7-0	Tx1 Power MSB	Internally measured Tx output optical power: unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm)	RO Opt.
155	7-0	Tx1 Power LSB		
156	7-0	Tx2 Power MSB		
157	7-0	Tx2 Power LSB		
158	7-0	Tx3 Power MSB		
159	7-0	Tx3 Power LSB		
160	7-0	Tx4 Power MSB		
161	7-0	Tx4 Power LSB		
162	7-0	Tx5 Power MSB		
163	7-0	Tx5 Power LSB		
164	7-0	Tx6 Power MSB		
165	7-0	Tx6 Power LSB		
166	7-0	Tx7 Power MSB		
167	7-0	Tx7 Power LSB		
168	7-0	Tx8 Power MSB		
169	7-0	Tx8 Power LSB		
170	7-0	Tx1 Bias MSB	Internally measured Tx bias current monitor: unsigned integer in 2 uA increments, times the multiplier from Table 8-33.	RO Opt.
171	7-0	Tx1 Bias LSB		
172	7-0	Tx2 Bias MSB		
173	7-0	Tx2 Bias LSB		
174	7-0	Tx3 Bias MSB		
175	7-0	Tx3 Bias LSB		
176	7-0	Tx4 Bias MSB		
177	7-0	Tx4 Bias LSB		
178	7-0	Tx5 Bias MSB		
179	7-0	Tx5 Bias LSB		
180	7-0	Tx6 Bias MSB		
181	7-0	Tx6 Bias LSB		
182	7-0	Tx7 Bias MSB		
183	7-0	Tx7 Bias LSB		
184	7-0	Tx8 Bias MSB		
185	7-0	Tx8 Bias LSB		
186	7-0	Rx1 Power MSB	Internally measured Rx input optical power: unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm)	RO Opt.
187	7-0	Rx1 Power LSB		
188	7-0	Rx2 Power MSB		
189	7-0	Rx2 Power LSB		
190	7-0	Rx3 Power MSB		
191	7-0	Rx3 Power LSB		
192	7-0	Rx4 Power MSB		
193	7-0	Rx4 Power LSB		

Byte	Bit	Name	Description	Type
194	7-0	Rx5 Power MSB		
195	7-0	Rx5 Power LSB		
196	7-0	Rx6 Power MSB		
197	7-0	Rx6 Power LSB		
198	7-0	Rx7 Power MSB		
199	7-0	Rx7 Power LSB		
200	7-0	Rx8 Power MSB		
201	7-0	Rx8 Power LSB		

8.8.4 Configuration Error Codes

The configuration requested by the host in either Staged Set may not be supported by the module for a variety of reasons. The Configuration Error Code registers are defined to provide feedback to the host software for cases where an invalid configuration was requested.

A code is provided for each lane (see Table 8-63). In cases where the feedback is data path-wide, the module shall populate all lanes in the data path with the same code. The applicable Configuration Error Code registers shall be populated by the module when the host sets one or more bits in Apply_DataPathInit or Apply_Immediate, before the requested configuration is copied into the Active Set. If the configuration was determined to be invalid by the module, the configuration shall not be copied into the Active Set. Any configuration error code greater than or equal to 2 indicates a rejected configuration.

Table 8-63 Configuration Error Code registers (Page 11h)

Byte	Bit	Name	Description	Type
202	7-4	Lane 2 Config Error Code	Configuration Error Code for lane 2	RO Opt.
	3-0	Lane 1 Config Error Code	Configuration Error Code for lane 1	
203	7-4	Lane 4 Config Error Code	Configuration Error Code for lane 4	RO Opt.
	3-0	Lane 3 Config Error Code	Configuration Error Code for lane 3	
204	7-4	Lane 6 Config Error Code	Configuration Error Code for lane 6	RO Opt.
	3-0	Lane 5 Config Error Code	Configuration Error Code for lane 5	
205	7-4	Lane 8 Config Error Code	Configuration Error Code for lane 8	RO Opt.
	3-0	Lane 7 Config Error Code	Configuration Error Code for lane 7	

Table 8-64 Configuration Error Codes (Page 11h)

Encoding	Name	Description
0h	No status	No status information available or config in process
1h	Config accepted	Configuration accepted and successfully applied
2h	Config rejected unknown	Configuration rejected for unknown reason
3h	Config rejected invalid code	Configuration rejected due to invalid ApSel Code request
4h	Config rejected invalid combo	Configuration rejected due to ApSel Code requested on invalid lane combination
5h	Config rejected invalid SI	Configuration rejected due to Invalid SI control set request
6h	Config rejected in use	Configuration rejected due to portion of lane group currently in use for a different Application (in order to switch to an Application with a different lane width, all lanes in the target Data Path must be in DataPathDeactivated)
7h	Config rejected incomplete lane info	DataPathInit requested with incomplete lane information
8h-Ch	Reserved	
Dh-Fh	Custom	Configuration rejected for custom reason

8.8.5 Active Control Set

The Active Control Set is required for all modules. Refer to section 6.2.3 for background on Control Set methodology.

Before exiting the MgmtInit state, the Active Control Set may be populated with a default Application Code and signal integrity settings. The host may update the Active Control Set by using the Apply_DataPathInit or Apply_Immediate control fields in either Staged Set 0 or Staged Set 1. See section 8.7.3 for a description of Control Set usage.

8.8.5.1 Application Select Fields

The following fields allow the host to infer the current baud rate, modulation format, and data path width for each lane in the module.

The ApSel Code shall be one of the module-advertised ApSel Codes from Table 8-13 or Table 8-39, or a value of 0000b to indicate that the applicable lane is not part of any data path. The Data Path code identifies the first lane in the data path. For example, a data path including lane 1 would be coded 000b and a data path where lane 5 is the lower lane number would be coded 100b. Explicit Control (bit 0 in bytes 206-213) indicates the host has specified signal integrity settings rather than using the Application-defined settings.

Table 8-65 Indicators for Active Control Set, Application Selected (Page 11h)

Byte	Bits	Name	Description	Type
206	7-4	Active Set Lane 1 ApSel code	ApSel Code from Table 8-13 or Table 8-39, lane 1	RO RQD
	3-1	Active Set Lane 1 Data Path ID	First lane in the data path containing lane 1 000b=Lane 1	
	0	Active Set Lane 1 Explicit Control	0b=Lane 1 settings are Application-defined 1b=Lane 1 settings are host-specified	
207	7-4	Active Set Lane 2 ApSel code	ApSel Code from Table 8-13 or Table 8-39, lane 2	RO RQD
	3-1	Active Set Lane 2 Data Path ID	First lane in the data path containing lane 2 000b=Lane 1, 001b=Lane 2	

Byte	Bits	Name	Description	Type
	0	Active Set Lane 2 Explicit Control	0b=Lane 2 settings are Application-defined 1b=Lane 2 settings are host-specified	
208	7-4	Active Set Lane 3 ApSel code	ApSel Code from Table 8-13 or Table 8-39, lane 3	RO RQD
	3-1	Active Set Lane 3 Data Path ID	First lane in the data path containing lane 3 000b=Lane 1, 001b=Lane 2, etc.	
	0	Active Set Lane 3 Explicit Control	0b=Lane 3 settings are Application-defined 1b=Lane 3 settings are host-specified	
209	7-4	Active Set Lane 4 ApSel code	ApSel Code from Table 8-13 or Table 8-39, lane 4	RO RQD
	3-1	Active Set Lane 4 Data Path ID	First lane in the data path containing lane 4 000b=Lane 1, 001b=Lane 2, etc.	
	0	Active Set Lane 4 Explicit Control	0b=Lane 4 settings are Application-defined 1b=Lane 4 settings are host-specified	
210	7-4	Active Set Lane 5 ApSel code	ApSel Code from Table 8-13 or Table 8-39, lane 5	RO RQD
	3-1	Active Set Lane 5 Data Path ID	First lane in the data path containing lane 5 000b=Lane 1, 001b=Lane 2, etc.	
	0	Active Set Lane 5 Explicit Control	0b=Lane 5 settings are Application-defined 1b=Lane 5 settings are host-specified	
211	7-4	Active Set Lane 6 ApSel code	ApSel Code from Table 8-13 or Table 8-39, lane 6	RO RQD
	3-1	Active Set Lane 6 Data Path ID	First lane in the data path containing lane 6 000b=Lane 1, 001b=Lane 2, etc.	
	0	Active Set Lane 6 Explicit Control	0b=Lane 6 settings are Application-defined 1b=Lane 6 settings are host-specified	
212	7-4	Active Set Lane 7 ApSel code	ApSel Code from Table 8-13 or Table 8-39, lane 7	RO RQD
	3-1	Active Set Lane 7 Data Path code	First lane in the data path containing lane 7 000b=Lane 1, 001b=Lane 2, etc.	
	0	Active Set Lane 7 Explicit Control	0b=Lane 7 settings are Application-defined 1b=Lane 7 settings are host-specified	
213	7-4	Active Set Lane 8 ApSel code	ApSel Code from Table 8-13 or Table 8-39, lane 8	RO RQD
	3-1	Active Set Lane 8 Data Path ID	First lane in the data path containing lane 8 000b=Lane 1, 001b=Lane 2, etc.	
	0	Active Set Lane 8 Explicit Control	0b=Lane 8 settings are Application-defined 1b=Lane 8 settings are host-specified	

8.8.5.2 Tx and Rx Signal Integrity Fields

The following fields allow the host to view the signal integrity settings for a lane. If the Explicit Control bit for a lane is set, the module is using the host-defined settings from Table 8-66 and Table 8-67. If the Explicit Control bit for a lane is clear, the module is using Application-defined default signal integrity settings. See section 6.2.4 for definitions of valid signal integrity control settings.

Table 8-66 Indicators for Active Control Set, Tx Controls (Page 11h)

Byte	Bits	Name	Description	Type
214	7	Active Set Tx8 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ) See Byte 220 Page 11h	RO Opt.
	6	Active Set Tx7 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ) See Byte 220 Page 11h	
	5	Active Set Tx6 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ) See Byte 219 Page 11h	
	4	Active Set Tx5 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ)	

Byte	Bits	Name	Description	Type
			See Byte 219 Page 11h	
	3	Active Set Tx4 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ) See Byte 218 Page 11h	
	2	Active Set Tx3 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ) See Byte 218 Page 11h	
	1	Active Set Tx2 Adaptive Input Eq Enable	1b=Enable 0b=Disable (use manual fixed EQ) See Byte 217 Page 11h	
	0	Active Set Tx1 Adaptive Input Eq Enable	1b=Enable 9 0b=Disable (use manual fixed EQ) See Byte 217 Page 11h	
215	7-6	Active Set Tx4 Adaptive Input Eq Recall	Recall stored Tx Eq adaptation value, 00b=do not recall 01b=store location 1 10b=store location 2 11b=reserved See Table 8-49 and Table 8-53	RO Opt.
	5-4	Active Set Tx3 Adaptive Input Eq Recall		
	3-2	Active Set Tx2 Adaptive Input Eq Recall		
	1-0	Active Set Tx1 Adaptive Input Eq Recall		
216	7-6	Active Set Tx8 Adaptive Input Eq Recall	Recall stored Tx Eq adaptation value, 00b=do not recall 01b=store location 1 10b=store location 2 11b=reserved See Table 8-49 and Table 8-53	RO Opt.
	5-4	Active Set Tx7 Adaptive Input Eq Recall		
	3-2	Active Set Tx6 Adaptive Input Eq Recall		
	1-0	Active Set Tx5 Adaptive Input Eq Recall		
217	7-4	Active Set Tx2 Input Eq control	Manual fixed Tx input eq control[1]	RO Opt.
	3-0	Active Set Tx1 Input Eq control	Manual fixed Tx input eq control[1]	
218	7-4	Active Set Tx4 Input Eq control	Manual fixed Tx input eq control[1]	RO Opt.
	3-0	Active Set Tx3 Input Eq control	Manual fixed Tx input eq control[1]	
219	7-4	Active Set Tx6 Input Eq control	Manual fixed Tx input eq control[1]	RO Opt.
	3-0	Active Set Tx5 Input Eq control	Manual fixed Tx input eq control[1]	
220	7-4	Active Set Tx8 Input Eq control	Manual fixed Tx input eq control[1]	RO Opt.
	3-0	Active Set Tx7 Input Eq control	Manual fixed Tx input eq control[1]	
221	7	Active Set Tx8 CDR control	1b=CDR enabled, 0b=CDR bypassed	RO Opt.
	6	Active Set Tx7 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	5	Active Set Tx6 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	4	Active Set Tx5 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	3	Active Set Tx4 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	2	Active Set Tx3 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	1	Active Set Tx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	0	Active Set Tx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	

Note 1: See Table 6-4

Table 8-67 Indicators for Active Control Set, Rx Controls (Page 11h)

Byte	Bits	Name	Description	Type
222	7	Active Set Rx8 CDR control	1b=CDR enabled, 0b=CDR bypassed	RO Opt.
	6	Active Set Rx7 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	5	Active Set Rx6 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	4	Active Set Rx5 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	3	Active Set Rx4 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	2	Active Set Rx3 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	1	Active Set Rx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	0	Active Set Rx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	
223	7-4	Active Set Rx2 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	RO Opt.
	3-0	Active Set Rx1 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	
224	7-4	Active Set Rx4 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	RO Opt.
	3-0	Active Set Rx3 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	
225	7-4	Active Set Rx6 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	RO Opt.
	3-0	Active Set Rx5 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	
226	7-4	Active Set Rx8 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	RO Opt.
	3-0	Active Set Rx7 Output Eq control, pre-cursor	Rx output equalization pre-cursor[1]	
227	7-4	Active Set Rx2 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	RO Opt.
	3-0	Active Set Rx1 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	
228	7-4	Active Set Rx4 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	RO Opt.
	3-0	Active Set Rx3 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	
229	7-4	Active Set Rx6 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	RO Opt.
	3-0	Active Set Rx5 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	
230	7-4	Active Set Rx8 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	RO Opt.
	3-0	Active Set Rx7 Output Eq control, post-cursor	Rx output equalization post-cursor[1]	
231	7-4	Active Set Rx2 Output Amplitude control	Rx output amplitude encoding[2]	RO Opt.
	3-0	Active Set Rx1 Output Amplitude control	Rx output amplitude encoding[2]	
232	7-4	Active Set Rx4 Output Amplitude control	Rx output amplitude encoding[2]	RO Opt.
	3-0	Active Set Rx3 Output Amplitude control	Rx output amplitude encoding[2]	
233	7-4	Active Set Rx6 Output Amplitude control	Rx output amplitude encoding[2]	RO Opt.
	3-0	Active Set Rx5 Output Amplitude control	Rx output amplitude encoding[2]	
234	7-4	Active Set Rx8 Output Amplitude control	Rx output amplitude encoding[2]	RO Opt.
	3-0	Active Set Rx7 Output Amplitude control	Rx output amplitude encoding[2]	
235-239		Reserved		RO

Note 1: See Table 6-5
Note 2: See Table 6-6

8.8.6 Module Media Lane to Module Media Wavelength and Fiber Mapping

Table 8-68 contains the advertising fields to define the mapping of module media lanes to module media wavelengths and physical fibers for muxed or WDM implementations. For WDM applications the shortest wavelength is always designated media wavelength 1 and starting from shortest wavelength through the longest all others are listed consecutively. The fiber numbers and names used in Table 8-68 are as defined in the appropriate hardware specification. See the relevant hardware specification and Table 8-13, Table 8-23 and Table 8-24 within for mapping constraints. Any mapping advertised in Table 8-68 that violates any of these constraints will not be a valid mapping.

Table 8-68 Module Media Lane to Module Media Wavelength and Fiber mapping (Page 11h)

Byte	Bits	Name	Description	Type
240	7-4	Module Tx media lane 1 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module Tx media lane 1 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or TR1 0010= Maps to module media fiber 2 or RT1 0011= Maps to module media fiber 3 or TR2 0100= Maps to module media fiber 4 or RT2 0101= Maps to module media fiber 5 or TR3 0110= Maps to module media fiber 6 or RT3 0111= Maps to module media fiber 7 or TR4 1000= Maps to module media fiber 8 or RT4 1001-1111= Reserved	
241	7-4	Module Tx media lane 2 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module Tx media lane 2 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or TR1 0010= Maps to module media fiber 2 or RT1 0011= Maps to module media fiber 3 or TR2 0100= Maps to module media fiber 4 or RT2 0101= Maps to module media fiber 5 or TR3 0110= Maps to module media fiber 6 or RT3 0111= Maps to module media fiber 7 or TR4 1000= Maps to module media fiber 8 or RT4 1001-1111= Reserved	
242	7-4	Module Tx media lane 3 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module Tx media lane 3 fiber mapping	0000= Mapping unknown or undefined	

Byte	Bits	Name	Description	Type
			0001= Maps to module media fiber 1 or TR1 0010= Maps to module media fiber 2 or RT1 0011= Maps to module media fiber 3 or TR2 0100= Maps to module media fiber 4 or RT2 0101= Maps to module media fiber 5 or TR3 0110= Maps to module media fiber 6 or RT3 0111= Maps to module media fiber 7 or TR4 1000= Maps to module media fiber 8 or RT4 1001-1111= Reserved	
243	7-4	Module Tx media lane 4 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module Tx media lane 4 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or TR1 0010= Maps to module media fiber 2 or RT1 0011= Maps to module media fiber 3 or TR2 0100= Maps to module media fiber 4 or RT2 0101= Maps to module media fiber 5 or TR3 0110= Maps to module media fiber 6 or RT3 0111= Maps to module media fiber 7 or TR4 1000= Maps to module media fiber 8 or RT4 1001-1111= Reserved	
244	7-4	Module Tx media lane 5 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module Tx media lane 5 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or TR1 0010= Maps to module media fiber 2 or RT1 0011= Maps to module media fiber 3 or TR2 0100= Maps to module media fiber 4 or RT2 0101= Maps to module media fiber 5 or TR3 0110= Maps to module media fiber 6 or RT3 0111= Maps to module media fiber 7 or TR4 1000= Maps to module media fiber 8 or RT4 1001-1111= Reserved	
245	7-4	Module Tx media lane 6 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4	RO Opt.

Byte	Bits	Name	Description	Type
			0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	
	3-0	Module Tx media lane 6 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or TR1 0010= Maps to module media fiber 2 or RT1 0011= Maps to module media fiber 3 or TR2 0100= Maps to module media fiber 4 or RT2 0101= Maps to module media fiber 5 or TR3 0110= Maps to module media fiber 6 or RT3 0111= Maps to module media fiber 7 or TR4 1000= Maps to module media fiber 8 or RT4 1001-1111= Reserved	
246	7-4	Module Tx media lane 7 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module Tx media lane 7 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or TR1 0010= Maps to module media fiber 2 or RT1 0011= Maps to module media fiber 3 or TR2 0100= Maps to module media fiber 4 or RT2 0101= Maps to module media fiber 5 or TR3 0110= Maps to module media fiber 6 or RT3 0111= Maps to module media fiber 7 or TR4 1000= Maps to module media fiber 8 or RT4 1001-1111= Reserved	
247	7-4	Module Tx media lane 8 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module Tx media lane 8 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or TR1 0010= Maps to module media fiber 2 or RT1 0011= Maps to module media fiber 3 or TR2 0100= Maps to module media fiber 4 or RT2 0101= Maps to module media fiber 5 or TR3 0110= Maps to module media fiber 6 or RT3 0111= Maps to module media fiber 7 or TR4 1000= Maps to module media fiber 8 or RT4	

Byte	Bits	Name	Description	Type
			1001-1111= Reserved	
248	7-4	Module Rx media lane 1 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module Rx media lane 1 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or RT1 0010= Maps to module media fiber 2 or TR1 0011= Maps to module media fiber 3 or RT2 0100= Maps to module media fiber 4 or TR2 0101= Maps to module media fiber 5 or RT3 0110= Maps to module media fiber 6 or TR3 0111= Maps to module media fiber 7 or RT4 1000= Maps to module media fiber 8 or TR4 1001-1111= Reserved	
249	7-4	Module Rx media lane 2 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module Rx media lane 2 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or RT1 0010= Maps to module media fiber 2 or TR1 0011= Maps to module media fiber 3 or RT2 0100= Maps to module media fiber 4 or TR2 0101= Maps to module media fiber 5 or RT3 0110= Maps to module media fiber 6 or TR3 0111= Maps to module media fiber 7 or RT4 1000= Maps to module media fiber 8 or TR4 1001-1111= Reserved	
250	7-4	Module Rx media lane 3 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module Rx media lane 3 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or RT1 0010= Maps to module media fiber 2 or TR1	

Byte	Bits	Name	Description	Type
			0011= Maps to module media fiber 3 or RT2 0100= Maps to module media fiber 4 or TR2 0101= Maps to module media fiber 5 or RT3 0110= Maps to module media fiber 6 or TR3 0111= Maps to module media fiber 7 or RT4 1000= Maps to module media fiber 8 or TR4 1001-1111= Reserved	
251	7-4	Module Rx media lane 4 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module Rx media lane 4 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or RT1 0010= Maps to module media fiber 2 or TR1 0011= Maps to module media fiber 3 or RT2 0100= Maps to module media fiber 4 or TR2 0101= Maps to module media fiber 5 or RT3 0110= Maps to module media fiber 6 or TR3 0111= Maps to module media fiber 7 or RT4 1000= Maps to module media fiber 8 or TR4 1001-1111= Reserved	
252	7-4	Module Rx media lane 5 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module Rx media lane 5 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or RT1 0010= Maps to module media fiber 2 or TR1 0011= Maps to module media fiber 3 or RT2 0100= Maps to module media fiber 4 or TR2 0101= Maps to module media fiber 5 or RT3 0110= Maps to module media fiber 6 or TR3 0111= Maps to module media fiber 7 or RT4 1000= Maps to module media fiber 8 or TR4 1001-1111= Reserved	
253	7-4	Module Rx media lane 6 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6	RO Opt.

Byte	Bits	Name	Description	Type
			0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	
	3-0	Module Rx media lane 6 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or RT1 0010= Maps to module media fiber 2 or TR1 0011= Maps to module media fiber 3 or RT2 0100= Maps to module media fiber 4 or TR2 0101= Maps to module media fiber 5 or RT3 0110= Maps to module media fiber 6 or TR3 0111= Maps to module media fiber 7 or RT4 1000= Maps to module media fiber 8 or TR4 1001-1111= Reserved	
254	7-4	Module Rx media lane 7 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module Rx media lane 7 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or RT1 0010= Maps to module media fiber 2 or TR1 0011= Maps to module media fiber 3 or RT2 0100= Maps to module media fiber 4 or TR2 0101= Maps to module media fiber 5 or RT3 0110= Maps to module media fiber 6 or TR3 0111= Maps to module media fiber 7 or RT4 1000= Maps to module media fiber 8 or TR4 1001-1111= Reserved	
255	7-4	Module Rx media lane 8 wavelength mapping	0000= Mapping unknown or undefined 0001= Maps to module media wavelength 1 0010= Maps to module media wavelength 2 0011= Maps to module media wavelength 3 0100= Maps to module media wavelength 4 0101= Maps to module media wavelength 5 0110= Maps to module media wavelength 6 0111= Maps to module media wavelength 7 1000= Maps to module media wavelength 8 1001-1111= Reserved	RO Opt.
	3-0	Module Rx media lane 8 fiber mapping	0000= Mapping unknown or undefined 0001= Maps to module media fiber 1 or RT1 0010= Maps to module media fiber 2 or TR1 0011= Maps to module media fiber 3 or RT2 0100= Maps to module media fiber 4 or TR2 0101= Maps to module media fiber 5 or RT3 0110= Maps to module media fiber 6 or TR3 0111= Maps to module media fiber 7 or RT4 1000= Maps to module media fiber 8 or TR4 1001-1111= Reserved	

8.9 Page 12h (Tuneable Laser Control and Status)

Upper memory Page 12h (Banked, with each bank referring to 8 media lanes) is used for Laser tuning, status and flags for transmitters with tunable technology. If Page 01h Byte 155 bit 6 is set to 1 (See Table 8-31 Implemented Controls Advertisement (Page 01h) , then this page is required to be supported. In multi-byte fields the lowest byte address represents lane 1. In single byte registers bit 0 represents lane 1.

Table 8-65 Laser tuning, status and flags for tunable transmitters (Page 12h)

Byte	Bit	Name	Description	Type
128-135	7-4	Lane 1-8 Selected Grid Spacing	Lane 1-8 selected grid spacing. Note that 1 byte is used for each lane. 0 = 3.125 GHz 1 = 6.25 GHz 2 = 12.5 GHz 3 = 25 GHz 4 = 50 GHz 5 = 100 GHz 6 = 75 GHz 7 = 33 GHz 8-14 = Reserved 15 = Not available	RW
	3-1	Reserved		RO
	0	Lane 1-8 Fine-tuning enable	Lane 1 fine-tuning enable. Note that 1 byte is used for each lane. 0b = Fine-tuning disabled 1b= Fine-tuning enabled.	RW
136-151	7-0	Lane 1-8 Channel Number	Lane 1-8 'n' tuning parameter. Each lane uses 2 Bytes, with a 16-bit signed representation. The 'n' parameter is defined based on the selected channel number. See page 04h for definitions relating to Frequency.	RW
152-167	7-0	Lane 1-8 Fine-tuning offset	Lane 1-8 fine-tuning frequency offset. Each lane uses 2 Bytes, with a 16-bit signed value in increments of 0.001 GHz.	RW
168-199	7-0	Lane 1-8 Current Laser Frequency	Lane 1-8 Current frequency. Each Lane uses 4 bytes in two 16-bit unsigned registers. The first (lowest 2 Bytes) is the frequency in THz units. Then 2nd (higher 2 Bytes) is in 0.05 GHz relative to the nearest THz. For example, if Lane 2 is currently reading 191.305 THz, then Byte 172-173 = 191, and Bytes 174-175 = 6100.	RO
200-215	7-0	Lane 1-8 Target output power	Lane 1-8 target programmable output power. Each Lane uses 2 Bytes 16-bit signed value in increments of 0.01 dBm	RW / Opt
216-222	7-0	Reserved		RO
223-229	7-2	Reserved		RO
	1	Lane 1-8 Tuning in Progress	Lane 1-8 laser tuning in progress real-time status flag. 0b = Tuning not in progress 1b = Tuning in progress	RO
	0	Lane 1-8 Wavelength Unlocked	Lane 1-8 laser wavelength unlocked real-time status flag. 0b = Wavelength locked 1b = Wavelength unlocked	RO
230	7-0	Lane 1-8 Laser Tuned Summary	Lanes Tx 1-8 latched laser tuned summary. 1 bit per Lane. Bit 0 corresponds to Lane 1. The bit will read as 1 when any of the latched bits in Bytes 231-238 are 1 for the particular Lane. It will clear to 0 when all of the corresponding bits in Bytes 231-238 are 0 for the particular Lane.	RO

Byte	Bit	Name	Description	Type
			The host should react to an interrupt by reading this Byte to indicate which Lane(s) are responsible for the interrupt. The host should then read the corresponding Lane Byte (231-238) to determine the specific interrupt and to clear the latch.	
231-238	7-4	Reserved		RO
	3	L-Lane 1-8 Tuning Busy	Lane 1-8 Latched flag indicating new channel change was attempted to be written while tuning was in process. Clear on read	RO
	2	L-Lane 1-8 Invalid Channel	Lane 1-8 Latched flag indicating 'n' was outside the advertised min/max channel range for the selected spacing. Clear on read	RO
	1	L-Lane 1-8 Latched Wavelength unlocked	Lane 1-8 Latched version of wavelength unlocked real-time status flag. Clear on read	RO
	0	L-Lane 1-8 Latched Tuning complete	Lane 1-8 Latched flag indicating laser tuning has been completed. Clear on read	RO
239-246	7-4	Reserved		RO
	3	M-Lane 1-8 Tuning Busy	Lane 1-8 interrupt mask for tuning busy flag	RW
	2	M-Lane 1-8 Invalid Channel	Lane 1-8 interrupt mask for invalid channel flag	RW
	1	M-Lane 1-8 Latched Wavelength unlocked	Lane 1-8 interrupt mask for wavelength unlocked flag	RW
	0	M-Lane 1-8 Latched Tuning complete	Lane 1-8 interrupt mask for tuning complete flag	RW
247-255	7-0	Reserved		RO

8.10 Page 13h (Module Diagnostics 1)

Upper memory map pages 13h and 14h are banked pages that contain module diagnostic control and status fields. The presence of Page 13h is conditional on the state of bit 5 in Page 01h byte 142 (see Table 8-28). Upper page 13h is subdivided into several areas as illustrated in the following table:

Table 8-66 Page 13h Overview

Byte	Size (bytes)	Name	Description
128	1	Loopback capabilities	Module advertisement
129	1	General pattern capabilities	Module advertisement
130	1	Diagnostic reporting capabilities	Module advertisement
131	1	Pattern Generation and Checking locations	Module advertisement
132-142	11	Pattern Generation and Checking capabilities	Module advertisement
143	1	Reserved	Reserved for Module advertisement
144-151	8	Pattern Generator, host side	Host controls
152-159	8	Pattern Generator, media side	Host controls
160-167	8	Pattern Checker, host side	Host controls
168-175	8	Pattern Checker, media side	Host controls
176-179	4	General Generator/Checker controls	Host controls
180-183	4	Loopback controls	Host controls
184-195	12	Reserved	
196-205	10	Custom	
206-223	18	Diagnostic flag masks	Page 14h Flags in bytes 132-149
224-255	32	User Pattern	

8.10.1 Loopback Capabilities Advertisement

Four different types of loopback are defined by this specification. Figure 8-3 illustrates each type.

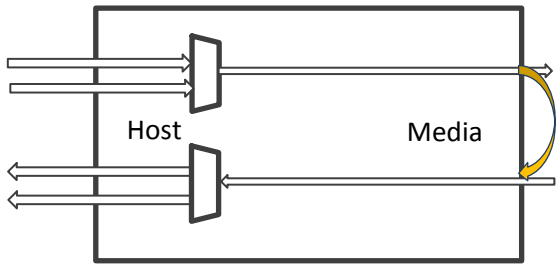
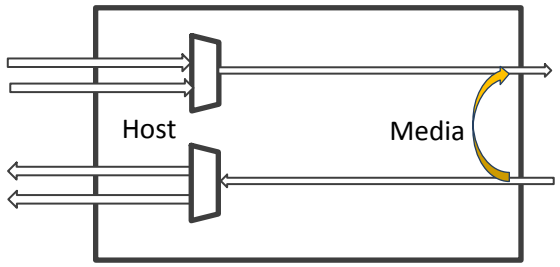
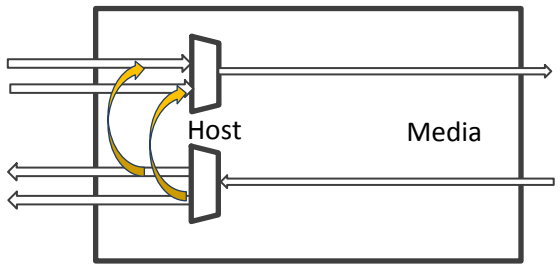
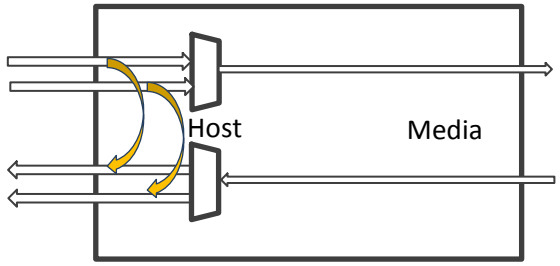
Name	Illustration
Media Side Output Loopback (only one host lane shown)	
Media Side Input Loopback (only one media lane shown)	
Host Side Output Loopback (only one media lane shown)	
Host Side Input Loopback (only one host lane shown)	

Figure 8-3 Loopback Type Illustrations

The loopback capabilities of the module are advertised in Table 8-69.

Table 8-69 Loopback Capabilities (Page 13h)

Byte	Bits	Name	Description	Type
128	7	Reserved		RO
	6	Simultaneous Host and Media Side Loopback supported	0b=Simultaneous host and media side loopback not supported 1b=Simultaneous host/media side loopback supported	RQD
	5	Per-lane Media Side Loopback supported	0b=Individual lane media side loopback not supported 1b=Individual lane media side loopback supported	
	4	Per-lane Host Side Loopback supported	0b=Individual lane host side loopback not supported 1b=Individual lane host side loopback supported	
	3	Host Side Input Loopback supported	0b=Host side input loopback not supported 1b=Host side input loopback supported	
	2	Host Side Output Loopback supported	0b=Host side output loopback not supported 1b=Host side output loopback supported	
	1	Media Side Input Loopback supported	0b=Media side input loopback not supported 1b=Media side input loopback supported	
	0	Media Side output Loopback supported	0b=Media side output loopback not supported 1b=Media side output loopback supported	

8.10.2 General Pattern Capabilities Advertisement

The general pattern generator/checker capabilities of the module are advertised in Table 8-70.

Table 8-70 General Pattern Capabilities (Page 13h)

Byte	Bits	Name	Description	Type
129	7-6	Gating Supported	00b=Not Supported 01b=Supported with time accuracy <= 2 ms 10b=Supported with time accuracy <= 20 ms 11b=Supported with time accuracy > 20 ms Total bits can be used to denote time, unless BER registers are used	RO RQD
	5	Latched Error Information Supported	Latched Error Information in Page 14h.Byte128 Selectors 11h-15h support advertisement. 0b=Not Supported. 1b=Supported.	
	4	Real-time BER Error Count Polling by Module	This flag controls if the module polls and updates the error information BER or Total Error Counters. Non-Gating Mode. 0b: Module does not poll Error Information. 1b: Module polls error information at update rate defined by 13h.Byte177.Bit0. Gating Mode. 0b: Modules does not poll Error Information. At the end of the gating period, the error counters are updated. If latched selectors 11h-15h are implemented these latched error counters will also be updated. 1b: Module Error Information is updated whilst Gating is in progress. Update time defined by Byte 177 Bit 0.	
	3	Per Lane Gating Timer	0b=One gating timer supported Host PRBS Checker and One Gating timer for Media PRBS Checkers is available for all lanes all banks. Two timers in totality. 1b=Per lane gating timer supported.	
	2	Auto Restart Implemented	0b=Auto Restart not implemented 1b=Auto Restart implemented.	
	1-0	Reserved	Reserved	

8.10.3 Diagnostic Reporting Capabilities Advertisement

The diagnostic reporting capabilities of the module are advertised in Table 8-70.

Table 8-70 Diagnostic Reporting Capabilities (Page 13h)

Byte	Bits	Name	Description	Type
130	7	Media side FEC supported	1b=Supported 0b=Not supported	RO RQD
	6	Host side FEC supported	1b=Supported 0b=Not supported	
	5	Media side input SNR measurement supported	Indicates if a Diagnostics Selection value of 09h is supported (Page 14h byte 128, Table 8-92) 1b=Supported 0b=Not supported	
	4	Host side input SNR measurement supported	Indicates if a Diagnostics Selection value of 08h is supported (Page 14h byte 128, Table 8-92) 1b=Supported 0b=Not supported	
	3	Media side input peak detector measurement supported	Indicates if a Diagnostics Selection value of 07h is supported (Page 14h byte 128, Table 8-92) 1b=Supported 0b=Not supported	
	2	Host side input peak detector measurement supported	Indicates if a Diagnostics Selection value of 06h is supported (Page 14h byte 128, Table 8-92) 1b=Supported 0b=Not supported	
	1	BER Error Count/Total Bits supported	Indicates if a Diagnostics Selection values of 02h-05h are supported (Page 14h byte 128, Table 8-92) 1b=Supported 0b=Not supported Some modules are unable to perform a 64 bit division to calculate and present BER. It is expected these types of module will present the BER as error counts and total bits elapsed for the error counts presented. Module should ensure data coherency of the 64 bit counters. Non-coherent counters may be detected as non-monotonic counts where the 64 bit counts are from two different samples in time. 64 bit coherency may require double buffering of the register data.	
	0	BER register supported	Indicates if a Diagnostics Selection value of 01h is supported (Page 14h byte 128, Table 8-92) 1b=Supported 0b=Not supported	

8.10.4 Pattern Generation and Checking Location Advertisement

The locations of PRBS generators, checkers and FEC functions are advertised in Table 8-71. A reference diagram showing the possible locations for PRBS generators, checkers and FEC functions is shown in Figure 8-4. The FEC block functionality is determined by the interface ID. (See SFF-8024)

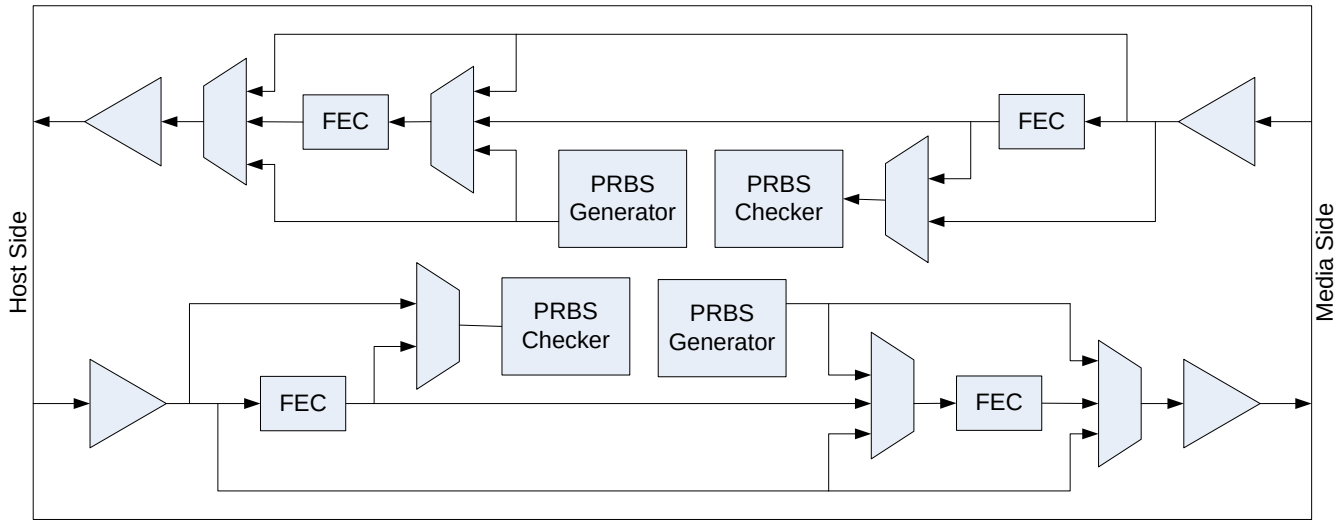


Figure 8-4 PRBS Paths Reference Diagram

Table 8-71 Pattern Generation and Checking Location (Page 13h)

Byte	Bits	Name	Description	Type
131	7	Media side pre-FEC PRBS generator supported	1b=Supported 0b=Not supported	RO RQD
	6	Media side post-FEC PRBS generator supported		
	5	Media side pre-FEC PRBS checker supported		
	4	Media side post-FEC PRBS checker supported		
	3	Host side pre-FEC PRBS generator supported		
	2	Host side post-FEC PRBS generator supported		
	1	Host side pre-FEC PRBS checker supported		
	0	Host side post-FEC PRBS checker supported		

8.10.5 Pattern Generation and Checking Capabilities Advertisement

This specification defines sixteen unique patterns that can be generated and/or checked by the module. These patterns are coded according to Table 8-72. All patterns with names ending in 'Q' are defined for PAM4 modulation using Gray coding. See section 3.3 for definition of Gray coding. The signal rate for these patterns is determined by the selected Application code for the associated lane.

Table 8-72 Pattern coding

PRBS Pattern code	Name	Description
0	PRBS-31Q	As defined in 802.3-2018 clause 120.5.11.2.2
1	PRBS-31	
2	PRBS-23Q	ITU-T Recommendation O.172, 2005
3	PRBS-23	
4	PRBS-15Q	x^15 + x^14 + 1
5	PRBS-15	
6	PRBS-13Q	As defined in 802.3-2018 clause 120.5.11.2.1
7	PRBS-13	
8	PRBS-9Q	As defined in 802.3-2018 clause 120.5.11
9	PRBS-9	
10	PRBS-7Q	x^7 + x^6 + 1
11	PRBS-7	
12	SSPRQ	As defined in 802.3-2018 clause 120.5.11.2.3
13	Reserved	
14	Custom	Vendor Pattern
15	User Pattern	Pattern provided in bytes 224-255

The pattern generation capabilities of the module are advertised in Table 8-73. The pattern number corresponds to the pattern coding in Table 8-72.

Table 8-73 PRBS Pattern Generation Capabilities (Page 13h)

Byte	Bits	Name	Description	Type
132	7	Host Side Generator Pattern 7 supported	1b=Supported 0b=Not supported	RO RQD
	6	Host Side Generator Pattern 6 supported		
	5	Host Side Generator Pattern 5 supported		
	4	Host Side Generator Pattern 4 supported		
	3	Host Side Generator Pattern 3 supported		
	2	Host Side Generator Pattern 2 supported		
	1	Host Side Generator Pattern 1 supported		
	0	Host Side Generator Pattern 0 supported		
133	7	Host Side Generator Pattern 15 supported	1b=Supported 0b=Not supported	RO RQD
	6	Host Side Generator Pattern 14 supported		
	5	Host Side Generator Pattern 13 supported		
	4	Host Side Generator Pattern 12 supported		
	3	Host Side Generator Pattern 11 supported		
	2	Host Side Generator Pattern 10 supported		
	1	Host Side Generator Pattern 9 supported		
	0	Host Side Generator Pattern 8 supported		
134	7	Media Side Generator Pattern 7 supported	1b=Supported 0b=Not supported	RO RQD
	6	Media Side Generator Pattern 6 supported		
	5	Media Side Generator Pattern 5 supported		
	4	Media Side Generator Pattern 4 supported		
	3	Media Side Generator Pattern 3 supported		
	2	Media Side Generator Pattern 2 supported		
	1	Media Side Generator Pattern 1 supported		
	0	Media Side Generator Pattern 0 supported		
135	7	Media Side Generator Pattern 15 supported	1b=Supported 0b=Not supported	RO RQD
	6	Media Side Generator Pattern 14 supported		
	5	Media Side Generator Pattern 13 supported		
	4	Media Side Generator Pattern 12 supported		
	3	Media Side Generator Pattern 11 supported		
	2	Media Side Generator Pattern 10 supported		
	1	Media Side Generator Pattern 9 supported		
	0	Media Side Generator Pattern 8 supported		

The pattern checking capabilities of the module are advertised in Table 8-74. The pattern number corresponds to the pattern coding in Table 8-72.

Table 8-74 Pattern Checking Capabilities (Page 13h)

Byte	Bits	Name	Description	Type
136	7	Host Side Checker Pattern 7 supported	1b=Supported 0b=Not supported	RO RQD
	6	Host Side Checker Pattern 6 supported		
	5	Host Side Checker Pattern 5 supported		
	4	Host Side Checker Pattern 4 supported		
	3	Host Side Checker Pattern 3 supported		
	2	Host Side Checker Pattern 2 supported		
	1	Host Side Checker Pattern 1 supported		
	0	Host Side Checker Pattern 0 supported		
137	7	Host Side Checker Pattern 15 supported	1b=Supported 0b=Not supported	RO RQD
	6	Host Side Checker Pattern 14 supported		
	5	Host Side Checker Pattern 13 supported		
	4	Host Side Checker Pattern 12 supported		
	3	Host Side Checker Pattern 11 supported		
	2	Host Side Checker Pattern 10 supported		
	1	Host Side Checker Pattern 9 supported		
	0	Host Side Checker Pattern 8 supported		
138	7	Media Side Checker Pattern 7 supported	1b=Supported 0b=Not supported	RO RQD
	6	Media Side Checker Pattern 6 supported		
	5	Media Side Checker Pattern 5 supported		
	4	Media Side Checker Pattern 4 supported		
	3	Media Side Checker Pattern 3 supported		
	2	Media Side Checker Pattern 2 supported		
	1	Media Side Checker Pattern 1 supported		
	0	Media Side Checker Pattern 0 supported		
139	7	Media Side Checker Pattern 15 supported	1b=Supported 0b=Not supported	RO RQD
	6	Media Side Checker Pattern 14 supported		
	5	Media Side Checker Pattern 13 supported		
	4	Media Side Checker Pattern 12 supported		
	3	Media Side Checker Pattern 11 supported		
	2	Media Side Checker Pattern 10 supported		
	1	Media Side Checker Pattern 9 supported		
	0	Media Side Checker Pattern 8 supported		

Additional pattern capabilities are advertised in Table 8-75.

Table 8-75 Pattern Generator and Checker swap and invert Capabilities (Page 13h)

Byte	Bits	Name	Description	Type
140	7-6	Recovered Clock can be used for pattern generator	00b:Recovered clock for generator not supported 01b:Supports Recovered clock pattern normal path 10b:Supports Recovered clock pattern loopback path. 11b:Supports both, selection made as function of loopback	RO RQD
	5	Reference Clock	Since this is the diagnostics page, the Reference clock bit here only controls reference clock in relation to diagnostics and not module operation. 1b:Reference Clock is available for patterns 0b:Reference Clock is not available for patterns	
	4-0	User Pattern supported length	Maximum length of the user pattern, in 2 byte increments. 0000b=2 bytes, 1111b=32 bytes	

Byte	Bits	Name	Description	Type
141	7	Media Side Checker Data Swap	0b: Page 13h.Byte170 not supported. 1b: Page 13h.Byte170 supported.	RO RQD
	6	Media Side Checker Data Invert	0b: Page 13h.Byte169 not supported. 1b: Page 13h.Byte169 sup6orted.	
	5	Media Side Generator Data Swap	0b: Page 13h.Byte154 not supported. 1b: Page 13h.Byte154 supported.	
	4	Media Side Generator Data Invert	0b: Page 13h.Byte153 not supported. 1b: Page 13h.Byte153 sup6orted.	
	3	Host Side Checker Data Swap	0b: Page 13h.Byte162 not supported. 1b: Page 13h.Byte162 supported.	
	2	Host Side Checker Data Invert	0b: Page 13h.Byte161 not supported. 1b: Page 13h.Byte161 sup6orted.	
	1	Host Side Generator Data Swap	0b: Page 13h.Byte146 not supported. 1b: Page 13h.Byte145 supported.	
	0	Host Side Generator Data Invert	0b: Page 13h.Byte145 not supported. 1b: Page 13h.Byte145 sup6orted.	
142	7	Media Checker Per lane Enables	Media Side pattern checker can be enable per lane at a time or all lanes will be enable. (13h.Byte168) 0b: per lane enable not supported. 1b: per lane enable supported.	RO RQD
	6	Media Checker Per Lane Pattern Type Selection	Media Side pattern checker type configuration. 0b: Pattern Type 13h.Byte172.3-0 applies to all lanes. 1b: Per lane Pattern Type 13h.Byte172-175.	
	5	Media Generator Per lane Enables	Media Side pattern generator can be enable per lane at a time or all lanes will be enable. (13h.Byte152) 0b: per lane enable not supported. 1b: per lane enable supported.	
	4	Media Generator Per Lane Pattern Type Selection	Media Side pattern checker type configuration. 0b: Pattern Type 13h.Byte156.3-0 applies to all lanes. 1b: Per lane Pattern Type 13h.Byte156-159.	
	3	Host Checker Per lane Enables	Host Side pattern checker can be enable per lane at a time or all lanes will be enable. (13h.Byte160) 0b: per lane enable not supported. 1b: per lane enable supported.	
	2	Host Checker Per Lane Pattern Type Selection	Host Side pattern checker type configuration. 0b: Pattern Type 13h.Byte164.3-0 applies to all lanes. 1b: Per lane Pattern Type 13h.Byte164-167.	
	1	Host Generator Per lane Enables	Host Side pattern generator can be enable per lane at a time or all lanes will be enable. (13h.Byte144) 0b: per lane enable not supported. 1b: per lane enable supported.	
	0	Host Generator Per Lane Pattern Type Selection	Host Side pattern checker type configuration. 0b: Pattern Type 13h.Byte148.3-0 applies to all lanes. 1b: Per lane Pattern Type 13h.Byte148-151.	
143	7-0	Reserved		RO RQD

8.10.6 Host Side Pattern Generator Controls

The controls in this section control pattern generation on the host side of the module, also known as the Rx electrical output.

Table 8-76 defines the host side pattern generator controls and Table 8-77 defines the host side pattern generator selection controls.

Table 8-76 Host Side Pattern Generator Controls (Page 13h)

Byte	Bits	Name	Description	Type
144	7	Host Side Generator Lane 8 enable	1b=Enable generator, using the configuration defined in bytes 145-151 0b=Disable pattern generator	RW Opt.
	6	Host Side Generator Lane 7 enable		
	5	Host Side Generator Lane 6 enable		
	4	Host Side Generator Lane 5 enable		
	3	Host Side Generator Lane 4 enable		
	2	Host Side Generator Lane 3 enable		
	1	Host Side Generator Lane 2 enable		
	0	Host Side Generator Lane 1 enable		
145	7	Host Side Generator Lane 8 data invert	1b=Invert the selected pattern 0b=Do not invert the selected pattern Note: This control inverts the pattern and does not swap the P and N signals. PN swap is controlled by the polarity controls in Table 8-46	RW Opt.
	6	Host Side Generator Lane 7 data invert		
	5	Host Side Generator Lane 6 data invert		
	4	Host Side Generator Lane 5 data invert		
	3	Host Side Generator Lane 4 data invert		
	2	Host Side Generator Lane 3 data invert		
	1	Host Side Generator Lane 2 data invert		
	0	Host Side Generator Lane 1 data invert		
146	7	Host Side Generator Lane 8 byte swap	1b=Swap the MSB and LSB for PAM4 patterns 0b=Do not swap MSB and LSB	RW Opt.
	6	Host Side Generator Lane 7 byte swap		
	5	Host Side Generator Lane 6 byte swap		
	4	Host Side Generator Lane 5 byte swap		
	3	Host Side Generator Lane 4 byte swap		
	2	Host Side Generator Lane 3 byte swap		
	1	Host Side Generator Lane 2 byte swap		
	0	Host Side Generator Lane 1 byte swap		
147	7	Host Side Generator Lane 8 pre-FEC enable	1b=Generate the selected pattern at the input to the internal FEC block 0b= Generate the selected pattern at the output from the internal FEC block	RW Opt.
	6	Host Side Generator Lane 7 pre-FEC enable		
	5	Host Side Generator Lane 6 pre-FEC enable		
	4	Host Side Generator Lane 5 pre-FEC enable		
	3	Host Side Generator Lane 4 pre-FEC enable		
	2	Host Side Generator Lane 3 pre-FEC enable		
	1	Host Side Generator Lane 2 pre-FEC enable		
	0	Host Side Generator Lane 1 pre-FEC enable		

Table 8-77 Host Side Pattern Generator Select Controls (Page 13h,)

Byte	Bits	Name	Description	Type
148	7-4	Host Side Generator Lane 2 pattern select	Selected pattern to be generated on each lane. See Table 8-72 for pattern codings.	RW Opt.
	3-0	Host Side Generator Lane 1 pattern select		
149	7-4	Host Side Generator Lane 4 pattern select		
	3-0	Host Side Generator Lane 3 pattern select		
150	7-4	Host Side Generator Lane 6 pattern select		
	3-0	Host Side Generator Lane 5 pattern select		
151	7-4	Host Side Generator Lane 8 pattern select		
	3-0	Host Side Generator Lane 7 pattern select		

8.10.7 Media Side Pattern Generator Controls

The controls in this section control pattern generation on the media side of the module, also known as the Tx electrical or optical output. Table 8-78 defines the media side pattern generator controls and Table 8-79 defines the media side pattern generator selection controls.

Table 8-78 Media Side Pattern Generator Controls (Page 13h)

Byte	Bits	Name	Description	Type
152	7	Media Side Generator Lane 8 enable	1b=Enable generator, using the configuration defined in bytes 153-159 0b=Disable pattern generator	RW Opt.
	6	Media Side Generator Lane 7 enable		
	5	Media Side Generator Lane 6 enable		
	4	Media Side Generator Lane 5 enable		
	3	Media Side Generator Lane 4 enable		
	2	Media Side Generator Lane 3 enable		
	1	Media Side Generator Lane 2 enable		
	0	Media Side Generator Lane 1 enable		
153	7	Media Side Generator Lane 8 data invert	1b=Invert the selected pattern 0b=Do not invert the selected pattern Note: This control inverts the pattern and does not swap the P and N signals. PN swap is controlled by the polarity controls in Table 8-46	RW Opt.
	6	Media Side Generator Lane 7 data invert		
	5	Media Side Generator Lane 6 data invert		
	4	Media Side Generator Lane 5 data invert		
	3	Media Side Generator Lane 4 data invert		
	2	Media Side Generator Lane 3 data invert		
	1	Media Side Generator Lane 2 data invert		
	0	Media Side Generator Lane 1 data invert		
154	7	Media Side Generator Lane 8 byte swap	1b=Swap the MSB and LSB for PAM4 patterns 0b=Do not swap MSB and LSB	RW Opt.
	6	Media Side Generator Lane 7 byte swap		
	5	Media Side Generator Lane 6 byte swap		
	4	Media Side Generator Lane 5 byte swap		
	3	Media Side Generator Lane 4 byte swap		
	2	Media Side Generator Lane 3 byte swap		
	1	Media Side Generator Lane 2 byte swap		
	0	Media Side Generator Lane 1 byte swap		
155	7	Media Side Generator Lane 8 pre-FEC enable	1b=Generate the selected pattern at the input to the internal FEC block 0b= Generate the selected pattern at the output from the internal FEC block	RW Opt.
	6	Media Side Generator Lane 7 pre-FEC enable		
	5	Media Side Generator Lane 6 pre-FEC enable		
	4	Media Side Generator Lane 5 pre-FEC enable		
	3	Media Side Generator Lane 4 pre-FEC enable		
	2	Media Side Generator Lane 3 pre-FEC enable		
	1	Media Side Generator Lane 2 pre-FEC enable		
	0	Media Side Generator Lane 1 pre-FEC enable		

Table 8-79 Media Side Pattern Generator Select Controls (Page 13h)

Byte	Bits	Name	Description	Type
156	7-4	Media Side Generator Lane 2 pattern select	Selected pattern to be generated on each lane. See Table 8-72 for pattern codings.	RW Opt.
	3-0	Media Side Generator Lane 1 pattern select		
157	7-4	Media Side Generator Lane 4 pattern select		
	3-0	Media Side Generator Lane 3 pattern select		
158	7-4	Media Side Generator Lane 6 pattern select		
	3-0	Media Side Generator Lane 5 pattern select		
159	7-4	Media Side Generator Lane 8 pattern select		
	3-0	Media Side Generator Lane 7 pattern select		

8.10.8 Host Side Pattern Checker Controls

The controls in this section control pattern checking on the host side of the module, also known as the Tx electrical input. Table 8-80 defines the host side pattern checker controls and Table 8-81 defines the host side pattern checker selection controls.

Table 8-80 Host Side Pattern Checker Controls (Page 13h)

Byte	Bits	Name	Description	Type
160	7	Host Side Checker Lane 8 enable	1b=Enable checker, using the configuration defined in bytes 161-167 0b=Disable pattern checker	RW Opt.
	6	Host Side Checker Lane 7 enable		
	5	Host Side Checker Lane 6 enable		
	4	Host Side Checker Lane 5 enable		
	3	Host Side Checker Lane 4 enable		
	2	Host Side Checker Lane 3 enable		
	1	Host Side Checker Lane 2 enable		
	0	Host Side Checker Lane 1 enable		
161	7	Host Side Checker Lane 8 data invert	1b=Invert the selected pattern 0b=Do not invert the selected pattern Note: This control inverts the pattern and does not swap the P and N signals. PN swap for input signals is not currently supported by this specification.	RW Opt.
	6	Host Side Checker Lane 7 data invert		
	5	Host Side Checker Lane 6 data invert		
	4	Host Side Checker Lane 5 data invert		
	3	Host Side Checker Lane 4 data invert		
	2	Host Side Checker Lane 3 data invert		
	1	Host Side Checker Lane 2 data invert		
	0	Host Side Checker Lane 1 data invert		
162	7	Host Side Checker Lane 8 byte swap	1b=Swap the MSB and LSB for PAM4 patterns 0b=Do not swap MSB and LSB	RW Opt.
	6	Host Side Checker Lane 7 byte swap		
	5	Host Side Checker Lane 6 byte swap		
	4	Host Side Checker Lane 5 byte swap		
	3	Host Side Checker Lane 4 byte swap		
	2	Host Side Checker Lane 3 byte swap		
	1	Host Side Checker Lane 2 byte swap		
	0	Host Side Checker Lane 1 byte swap		
163	7	Host Side Checker Lane 8 post-FEC enable	1b=Check the selected pattern at the output from the internal FEC block 0b=Check the selected pattern at the input to the internal FEC block	RW Opt.
	6	Host Side Checker Lane 7 post-FEC enable		
	5	Host Side Checker Lane 6 post-FEC enable		
	4	Host Side Checker Lane 5 post-FEC enable		
	3	Host Side Checker Lane 4 post-FEC enable		
	2	Host Side Checker Lane 3 post-FEC enable		
	1	Host Side Checker Lane 2 post-FEC enable		
	0	Host Side Checker Lane 1 post-FEC enable		

Table 8-81 Host Side Pattern Checker Select Controls (Page 13h)

Byte	Bits	Name	Description	Type
164	7-4	Host Side Checker Lane 2 pattern select	Selected pattern to be generated on each lane. See Table 8-72 for pattern codings.	RW Opt.
	3-0	Host Side Checker Lane 1 pattern select		
165	7-4	Host Side Checker Lane 4 pattern select		
	3-0	Host Side Checker Lane 3 pattern select		
166	7-4	Host Side Checker Lane 6 pattern select		
	3-0	Host Side Checker Lane 5 pattern select		
167	7-4	Host Side Checker Lane 8 pattern select		
	3-0	Host Side Checker Lane 7 pattern select		

8.10.9 Media Side Pattern Checker Controls

The controls in this section control pattern checking on the media side of the module, also known as the Rx electrical or optical input. Table 8-82 defines the media side pattern checker controls and Table 8-83 defines the media side pattern checker selection controls.

Table 8-82 Media Side Pattern Checker Controls (Page 13h)

Byte	Bits	Name	Description	Type
168	7	Media Side Checker Lane 8 enable	1b=Enable checker, using the configuration defined in bytes 169-175 0b=Disable pattern checker	RW Opt.
	6	Media Side Checker Lane 7 enable		
	5	Media Side Checker Lane 6 enable		
	4	Media Side Checker Lane 5 enable		
	3	Media Side Checker Lane 4 enable		
	2	Media Side Checker Lane 3 enable		
	1	Media Side Checker Lane 2 enable		
	0	Media Side Checker Lane 1 enable		
169	7	Media Side Checker Lane 8 data invert	1b=Invert the selected pattern 0b=Do not invert the selected pattern Note: This control inverts the pattern and does not swap the P and N signals. PN swap for input signals is not currently supported by this specification.	RW Opt.
	6	Media Side Checker Lane 7 data invert		
	5	Media Side Checker Lane 6 data invert		
	4	Media Side Checker Lane 5 data invert		
	3	Media Side Checker Lane 4 data invert		
	2	Media Side Checker Lane 3 data invert		
	1	Media Side Checker Lane 2 data invert		
	0	Media Side Checker Lane 1 data invert		
170	7	Media Side Checker Lane 8 byte swap	1b=Swap the MSB and LSB for PAM4 patterns 0b=Do not swap MSB and LSB	RW Opt.
	6	Media Side Checker Lane 7 byte swap		
	5	Media Side Checker Lane 6 byte swap		
	4	Media Side Checker Lane 5 byte swap		
	3	Media Side Checker Lane 4 byte swap		
	2	Media Side Checker Lane 3 byte swap		
	1	Media Side Checker Lane 2 byte swap		
	0	Media Side Checker Lane 1 byte swap		
171	7	Media Side Checker Lane 8 post-FEC enable	1b=Check the selected pattern at the output from the internal FEC block 0b=Check the selected pattern at the input to the internal FEC block	RW Opt.
	6	Media Side Checker Lane 7 post-FEC enable		
	5	Media Side Checker Lane 6 post-FEC enable		
	4	Media Side Checker Lane 5 post-FEC enable		
	3	Media Side Checker Lane 4 post-FEC enable		
	2	Media Side Checker Lane 3 post-FEC enable		
	1	Media Side Checker Lane 2 post-FEC enable		
	0	Media Side Checker Lane 1 post-FEC enable		

Table 8-83 Media Side Pattern Checker Select Controls (Page 13h)

Byte	Bits	Name	Description	Type
172	7-4	Media Side Checker Lane 2 pattern select	Selected pattern to be generated on each lane. See Table 8-72 for pattern codings.	RW Opt.
	3-0	Media Side Checker Lane 1 pattern select		
173	7-4	Media Side Checker Lane 4 pattern select		
	3-0	Media Side Checker Lane 3 pattern select		
174	7-4	Media Side Checker Lane 6 pattern select		
	3-0	Media Side Checker Lane 5 pattern select		
175	7-4	Media Side Checker Lane 8 pattern select		
	3-0	Media Side Checker Lane 7 pattern select		

8.10.10 General Generator/Checker Controls

Table 8-84 provides general controls for the pattern generator and checker features. For examples of the usage of the Generator/Checker Controls see Appendix C.

Table 8-84 General Generator/Checker Controls (Page 13h)

Byte	Bits	Name	Description	Type
176	7-4	Host PRBS Generator Clock Source	The source of the clock to be that is used for Host PRBS Pattern Generation can be configured using this control register. The following selection options are defined. 0h:All lanes uses Internal Clock 1h:All lanes uses Reference Clock 2h:All lanes uses Recovered Clock Media Lane 1 3h:All lanes uses Recovered Clock Media Lane 2 4h:All lanes uses Recovered Clock Media Lane 3 5h:All lanes uses Recovered Clock Media Lane 4 6h:All lanes uses Recovered Clock Media Lane 5 7h:All lanes uses Recovered Clock Media Lane 6 8h:All lanes uses Recovered Clock Media Lane 7 9h:All lanes uses Recovered Clock Media Lane 8 Ah-Eh: Reserved. Fh: Recovered clock from Respective Media Lane/Datapaths are used.	RW Opt.
	3-0	Media PRBS Generator Clock Source	The source of the clock to be that is used for Media PRBS Pattern Generation can be configured using this control register. The following selection options are defined. 0h:All lanes uses Internal Clock 1h:All lanes uses Reference Clock 2h:All lanes uses Recovered Clock Host Lane 1 3h:All lanes uses Recovered Clock Host Lane 2 4h:All lanes uses Recovered Clock Host Lane 3 5h:All lanes uses Recovered Clock Host Lane 4 6h:All lanes uses Recovered Clock Host Lane 5 7h:All lanes uses Recovered Clock Host Lane 6 8h:All lanes uses Recovered Clock Host Lane 7 9h:All lanes uses Recovered Clock Host Lane 8 Ah-Eh: Reserved. Fh: Recovered clock from Respective Host Lane/Datapaths are used.	
177	7	Reset all lanes	This bit controls the behavior of the “Reset Error	RW

Byte	Bits	Name	Description	Type
			Counters" or "Enabling and Disabling PRBS checker lanes", whether the operation applies to enabled lanes within a bank or enabled lanes in all banks with this bit set to 1b. 0b: Applies to individual lane/bank. 1b: Applies to all lanes all banks with this bit=1. Whenever a reset error information operation on and individual lane or all lanes are triggered, it should always clear Error Information (both PRBS BER and Error Counters) at the same time.	Opt.
	6	Reserved	Reserved	
	5	Reset Error Information	Whenever this bit is set to 1b, the Error Information in Selector 01h to 05h are frozen and if implemented 11h-15h will be updated with the Error Information. Whenever this bit is set to 0b, Error Information in Selectors 01h-05h will be reset to 0. Selectors 11h-15h will not be affected by this bit setting to 0. Furthermore, the behavior of this bit depends on the configuration 13h.Byte129.Bit3 and register 13h.Byte177.Bit7 as well as the Gating Mode 13h.Byte177.Bit3-1. When configuration in 13h.Byte129.Bit3=0, there is only 1 timer for all lane and all banks. Setting this bit to 1b will keep the gate timers reset. Setting this bit to 0b will start the single gating timer. When configuration 13h.Byte129.Bit3=1, there are individual timers per lane (in all banks). Setting this bit to 1b will keep the gate timers reset for the lanes in this bank only if 13h.Byte177.Bit7=0. Setting this bit to 0b will start the individual gating timers for all enabled lanes in this bank.	
	4	Auto Restart Gate Time	0b=When Gate Time expires, the module will set the Gate Complete Flag in Page 14h, bytes 134-135. The module will update the latched error counters and stop error detection. 1b=When Gate Time expires, the module will set the Gate Complete Flag in Page 14h, bytes 134-135. The module will update the latched error counters, then immediately clear internal error counters and restart the Gate Timer, while continuing to count errors. The host must read the latched error counters before the Gate Time expires to avoid the values being overwritten with new counts.	

Byte	Bits	Name	Description	Type
	3-1	Gate Time	The pattern checker will stop accumulating errors after this gate time has elapsed. 000b=not gated, counters accrue indefinitely 001b=5 sec gate time 010b=10 sec gate time 011b=30 sec gate time 100b=60 sec gate time 101b=120 sec gate time 110b=300 sec gate time 111b=Custom	
	0	BER/Error Count Update time	If configured (see Table 8-70) Page 13h Byte 129 Bit 4 when set to 1b advertises that the module will be able to update the BER or Error counters whilst gating is in progress. Two update rates at which the module will process the internal error counters and update the error counter fields in the memory map are possible. If gating is enabled, the host can poll error registers for cumulative “real-time” error counts, up until the first gate is reached. 0b=1 sec update interval 1b=5 sec update interval Data coherency shall be maintained by the module. For example on a 64-bit read, 8 bytes are transferred over TWI. The module shall ensure that the 8 bytes come from a discrete sample. A multi-byte read is required to ensure coherency.	
178	7-4	Reserved		RW
	3-2	Host PRBS Checker Clock Source	The source of the clock that is used for the Host PRBS Pattern Checker can be configured using this control register. The following selection options are defined. 0h: Recovered clocks from Respective Host Lane/Datapaths are used. 1h: All lanes use Internal Clock. 2h: All lanes use Reference Clock 3h: Reserved.	RW
	1-0	Media PRBS Checker Clock Source	The source of the clock that is used for the Media PRBS Pattern Checker can be configured using this control register. The following selection options are defined. 0h: Recovered clocks from Respective Media Lane/Datapaths are used. 1h: All lanes use Internal Clock. 2h: All lanes use Reference Clock 3h: Reserved.	RW
179	7-0	Reserved		RW

8.10.10.1 PRBS Controls and Behavior Un-Gated Mode

These section describes the behavior specifically related to behavior of the PRBS Checkers and error information registers when 13h.Byte177.Bits3-1 is 000b. The PRBS error information accessed by the selector byte Page 14h.Byte128 and information Bytes 192-255 will be referenced in the following table below. Furthermore the configuration of Page 13h.Byte129.Bit4 defines the behavior of the module availability of the real-time error information.

The COR flags in Page 14h.Bytes 134-135 will be not raised is this un-gated PRBS checker mode and the host will have to poll the error information registers.

Table 8-85 PRBS Checker Behavior Un-Gated Mode

Required Mode of Operation	Byte 177 (D7-D0)	Description
Bit 3-1=000b. Not-Gated (Hence Bit 4 ignored) All lanes control bit 7=0.	0000 000y *nnn* = 000	In this mode, the error information BER and error counters are running continuously. Whenever PRBS Enable Bits in Page 13h Byte/s 160 or 168 are enabled by TWI write, all error counters for the enable lanes will reset to 0 and start accumulating errors. PRBS Error counters are stopped when the host disables the PRBS Error Checker Bytes 160 or 168, at which time the error information of prior to disabled will be available in the Selector 01-05h and the module shall present the last error information in both the Selector 01h-05h (and 11h-15h if implemented). If 13h.Byte129.Bit4 = 0, real time error information are not updated. The error information will only available when the PRBS enable bits on Byte 160 or 168 are disabled. If 13h.Byte129.Bit4 = 1, real time error information are available by using Page 14h using the Selectors 01h-05h. These real time error information will be updated by the module every configure "y" seconds. Accurate error counter accumulation times can be derived from the total bit counters in the error information. A write to 13h.Byte177.Bit5=1 will also cause the error information registers to reset to 0 and restart accumulation on the enabled lanes.
Bit 3-1=000b. Not-Gated (Hence Bit 4 ignored) All lanes control bit 7=1.	100x 000y *nnn* = 000	The behavior with is the same as the above row with the exception that when a write to 13h.Byte177.Bit5=1 the error information registers of **all lanes in all banks** (since 13h.Byte177.Bit7=1) will be reset to 0 and restart accumulation. As described above just prior to reset of error information of all lanes in all banks, the previous error information should be copied to both 01-05h (and 11h-15h if implemented). Selector 01-05h will restart accumulation and 11h-15h if implemented will contain the latched error information of the previous period prior to reset.
Reset Error Counters (Bit 5) Since 13h.Byte129.Bit3=0 there is only one timer for host and one timer	x010 nnny nnn = 000	This bit is used to clear the error counters and restart accumulation of errors. When 13h.Byte177.Bit5 is set to 1b, all the enabled lanes error counters are frozen from the previous state and available from reading Selectors 01h-05h (and 11h-15h

Required Mode of Operation	Byte 177 (D7-D0)	Description
for media lanes. Hence 13h.Byte177.Bit7 has no relevance.		if implemented). When 13h.Byte177.Bit5 is set to 0b, all the error information of enabled PRBS checker of both host and media lanes are reset to 0. The host may also individually toggle Host Byte 160 or Media Byte 168 enable bits to restart the error information of the lanes independently.

8.10.10.2 PRBS Controls and Behavior – Single Gate Timer

These section describes the behavior specifically related to behavior of the module when Page 13h.Byte129.Bit3 is 0 indicating that there is only one Gate Timer for all channels and all banks. The PRBS error information accessed by the selector byte Page 14h.Byte128 and information Bytes 192-255 will be referenced in the following table below. Furthermore the configuration of Page 13h.Byte129.Bit4 defines the behavior of the module availability of the real-time error information whilst the gating timer is running and has not expired.

In the following table whenever gating is enabled, the COR flags in Page 14h.Bytes 134-135 will be raised as well as IntL may be asserted at the expiry of the gate timers to indicate that error information registers are available. If the host fails to read the error information registers prior to expiry of subsequent gate time expiry, only the latest error information will be available.

Table 8-86 PRBS Checker Behavior Single Gate Timer

Required Mode of Operation	Byte 177 (D7-D0)	Description
Gated, nnn configured secs. Since 13h.Byte129.Bit3=0 the control 13h.Byte177.Bit7 is ignored.	X000 *nnny* *nnn* != 000	PRBS Error Counters are gated. Whenever PRBS Enable Bits in Page 13h Byte/s 160 or 168 are enabled by TWI write, the respective Host or Media single gate timer will reset to 0, all error counters for the enable lanes will reset to 0 and start accumulating errors. At the end of the gate, that is when the gate timer expires and exceeds the “nnn” elapsed time configured seconds, the PRBS Error counters will stop counting. At this time the module shall be able to present the error information collected within this gating period on Page 14h by using the Selectors 01h-05h (and 11h-15h if implemented). If 13h.Byte129.Bit4 = 0, real time error information are not updated whilst gating is in progress. The error information will only available at the end of the gate. If 13h.Byte129.Bit4 = 1, real time error information are available by using Page 14h using the Selectors 01h-05h. These real time error information will be updated by the module every configure “y” seconds. This mode is useful if the gating period is long. A host may choose to periodically read the real-time error information during gating and take any necessary action if a bad BER is detected. To restart gating, the host has to toggle the PRBS enable registers 160 and 168.
Gated, nnn configured secs.	xx01 *nnny*	This behavior is the same as the above row, except for the

Required Mode of Operation	Byte 177 (D7-D0)	Description
Since 13h.Byte129.Bit3=0 the control 13h.Byte177.Bit7 is ignored. If the Page 13h.Byte129.Bit2 is set, and the host writes a 1 to Bit4 of Byte 177, the gating timer will automatically restart.	*nnn* != 000	behavior when the gate timer expires and exceeds the configured gate time. Module should support Selectors 11h-15h to use this feature, otherwise error information from the previous gating period will be lost. Here at the end of the gate, that is when the gate timer expires and exceeds the configured "nnn" elapsed time, the PRBS error information will be presented in the latched error information via the Selectors 11h-15h. The current error information will reset and the gate timer will be reset to 0 and restart accumulating errors for a new gating period. The host will have to read the error information from the previous gated time using the latched error information Selectors 11h-15h.
Restart gate timer (Bit 5) Since 13h.Byte129.Bit3=0 there is only one timer for host and one timer for media lanes. Hence 13h.Byte177.Bit7 has no relevance.	x01x *nnn*y *nnn* != 000	This bit is used to restart the both the single host and media gate timers. When Byte177.Bit5 is set to 1b, all the enabled lanes error counters are frozen from the previous state and the gate timers are stopped. When Byte177.Bit5 is set to 0b, both the host and media enabled the gate timers are restarted from 0 and the error information are reset and a new error accumulation gate period is restarted. The host may also individually toggle host Byte 160 or media Byte 168 enable bits to restart the gate timer for the host and media lanes independently.

8.10.10.3 PRBS Controls and Behavior – Per Lane Gate Timer

These section describes the behavior specifically related to behavior of the module when Page 13h.Byte129.Bit3 is 1 indicating that there are individual lanes Gate Timer for all channels and all banks. The PRBS error information accessed by the selector byte Page 14h.Byte128 and information Bytes 192-255 will be referenced in the following table below. Furthermore the configuration of Page 13h.Byte129.Bit4 defines the behavior of the module availability of the real-time error information whilst the gating timer is running and has not expired.

In the following table whenever gating is enabled, the COR flags in Page 14h.Bytes 134-135 will be raised as well as IntL may be asserted at the expiry of the gate timers to indicate that error information registers are available. If the host fails to read the error information registers prior to expiry of subsequent gate time expiry, only the latest error information will be available.

Table 8-87 PRBS Checker Behavior Per Lane Gate Timer

Required Mode of Operation	Byte 177 (D7-D0)	Description
Gated, nnn configured secs. Since 13h.Byte129.Bit3=0 the control 13h.Byte177.Bit7 is ignored.	X000 *nnn*y *nnn* != 000	PRBS Error Counters are gated. Whenever PRBS Enable Bits in Page 13h Byte/s 160 or 168 are enabled by TWI write, the respective Host or Media lane gate timer will reset to 0, all error counters for the enable lanes will reset to 0 and start accumulating errors. Since there are individual per lane gate timers, these timers should reset independently to provide the most accurate per lane gated time as possible. At the end of the gate, that is when the gate timer expires and exceeds the "nnn" elapsed time configured seconds, the PRBS

Required Mode of Operation	Byte 177 (D7-D0)	Description
		Error counters will stop counting. At this time the module shall be able to present the error information collected within this gating period on Page 14h by using the Selectors 01h-05h (and 11h-15h if implemented). If 13h.Byte129.Bit4 = 0, real time error information are not updated whilst gating is in progress. The error information will only available at the end of the gate. If 13h.Byte129.Bit4 = 1, real time error information are available by using Page 14h using the Selectors 01h-05h. These real time error information will be updated by the module every configure "y" seconds. This mode is useful if the gating period is long. A host may choose to periodically read the real-time error information during gating and take any necessary action if a bad BER is detected. To restart gating, the host has to toggle the PRBS enable registers 160 and 168 or set Page 13h.Byte177.Bit5.
Gated, nnn configured secs. Since 13h.Byte129.Bit3=0 the control 13h.Byte177.Bit7 is ignored. If the Page 13h.Byte129.Bit2 is set, and the host writes a 1 to Bit4 of Byte 177, the gating timer will automatically restart.	xx01 *nnny* *nnn* != 000	This behavior is the same as the above row, except for the behavior when the gate timer expires and exceeds the configured gate time. Module shall support Selectors 11h-15h to use this feature. Here at the end of the gate, that is when the individual per lane gate timer expires and exceeds the configured "nnn" elapsed time, the PRBS error information will be presented in the latched error information via the Selectors 11h-15h. The current error information will reset and the gate timer will be reset to 0 and restart accumulating errors for a new gating period. The host will have to read the error information from the previous gated time using the latched error information Selectors 11h-15h.
Restart gate timer (Bit 5)	x01x *nnny* *nnn* != 000	This bit is used to restart all the enabled bank and lanes gate timers. When Byte177.Bit5 is set to 1b, all the enabled lanes error counters are frozen from the previous state and the gate timers are stopped. If Byte177.Bit7=0, when Byte177.Bit5 is set to 0b, all the enabled the gate timers of the current selected bank are restarted from 0 and the error information are reset and a new error accumulation gate period is restarted. If Byte177.Bit7=1, when Byte177.Bit5 is set to 0b, all the enabled the gate timers of the all banks with Byte177.Bit7=1 are restarted from 0 and the error information are reset and a new error accumulation gate period is restarted. The host may also individually toggle host Byte 160 or media Byte 168 enable bits to restart the gate timer for the host and media lanes independently. In this case, only the error information of the enable or disabled lane will reset and start count or freeze in its last value respectively.

8.10.11 Loopback Controls

Host and Media side loopback control registers and module behaviors depend on the advertised loopback capabilities in Table 8-69. Table 8-88 provides controls for loopback features in the module. The host-written loopback settings may be rejected by the module. For example, if the module advertises that it can only perform host side or media side loopback one at a time and not simultaneously, the module may reject the command and the values in the loopback controls may not change.

Table 8-88 Loopback Controls (Page 13h)

Byte	Bits	Name	Description	Type
180	7	Media side output loopback lane 8 enable	0b=normal non-loopback operation 1b=loopback operation enabled. If the Per-lane Media Side Loopback Supported field=1, loopback control is per lane. Otherwise, if any loopback enable bit is set to 1, all Media side lanes are in output loopback.	RW Opt.
	6	Media side output loopback lane 7 enable		
	5	Media side output loopback lane 6 enable		
	4	Media side output loopback lane 5 enable		
	3	Media side output loopback lane 4 enable		
	2	Media side output loopback lane 3 enable		
	1	Media side output loopback lane 2 enable		
	0	Media side output loopback lane 1 enable		
181	7	Media side input loopback lane 8 enable	0b=normal non-loopback operation 1b=loopback operation enabled. If the Per-lane Media Side Loopback Supported field=1, loopback control is per lane. Otherwise, if any loopback enable bit is set to 1, all media side lanes are in input loopback.	RW Opt.
	6	Media side input loopback lane 7 enable		
	5	Media side input loopback lane 6 enable		
	4	Media side input loopback lane 5 enable		
	3	Media side input loopback lane 4 enable		
	2	Media side input loopback lane 3 enable		
	1	Media side input loopback lane 2 enable		
	0	Media side input loopback lane 1 enable		
182	7	Host side output loopback lane 8 enable	0b=normal non-loopback operation 1b=loopback operation enabled. If the Per-lane Host Side Loopback Supported field=1, loopback control is per lane. Otherwise, if any loopback enable bit is set to 1, all host side lanes are in output loopback.	RW Opt.
	6	Host side output loopback lane 7 enable		
	5	Host side output loopback lane 6 enable		
	4	Host side output loopback lane 5 enable		
	3	Host side output loopback lane 4 enable		
	2	Host side output loopback lane 3 enable		
	1	Host side output loopback lane 2 enable		
	0	Host side output loopback lane 1 enable		
183	7	Host side input loopback lane 8 enable	0b=normal non-loopback operation 1b=loopback operation enabled. If the Per-lane Host Side Loopback Supported field=1, loopback control is per lane. Otherwise, if any loopback enable bit is set to 1, all Host side lanes are in input loopback.	RW Opt.
	6	Host side input loopback lane 7 enable		
	5	Host side input loopback lane 6 enable		
	4	Host side input loopback lane 5 enable		
	3	Host side input loopback lane 4 enable		
	2	Host side input loopback lane 3 enable		
	1	Host side input loopback lane 2 enable		
	0	Host side input loopback lane 1 enable		

8.10.12 Diagnostics Flag Masks

Table 8-89 provides masking bits for all diagnostics flags. Diagnostics flags are located on Page 14h (see Table 8-93).

Table 8-89 Diagnostics Flag Masks (Page 13h)

Byte	Bits	Name	Description	Type
206	7	M-Loss of reference clock	Loss of reference clock flag mask for the module	R/W Opt.
	6-0	Reserved		
207	7-0	Reserved		R/W
208	7	M-Host Lane 8 Pattern Checker Gating Complete	Per-host lane gating complete flag mask. When gating is complete, this bit will be set to 1. These bits will be cleared upon pattern checker reset or disable.	R/W Opt.
	6	M-Host Lane 7 Pattern Checker Gating Complete		
	5	M-Host Lane 6 Pattern Checker Gating Complete		
	4	M-Host Lane 5 Pattern Checker Gating Complete		
	3	M-Host Lane 4 Pattern Checker Gating Complete		
	2	M-Host Lane 3 Pattern Checker Gating Complete		
	1	M-Host Lane 2 Pattern Checker Gating Complete		
	0	M-Host Lane 1 Pattern Checker Gating Complete		
209	7	M-Media Lane 8 Pattern Checker Gating Complete	Per-media lane gating complete flag mask. When gating is complete, this bit will be set to 1. These bits will be cleared upon pattern checker reset or disable.	R/W Opt.
	6	M-Media Lane 7 Pattern Checker Gating Complete		
	5	M-Media Lane 6 Pattern Checker Gating Complete		
	4	M-Media Lane 5 Pattern Checker Gating Complete		
	3	M-Media Lane 4 Pattern Checker Gating Complete		
	2	M-Media Lane 3 Pattern Checker Gating Complete		
	1	M-Media Lane 2 Pattern Checker Gating Complete		
	0	M-Media Lane 1 Pattern Checker Gating Complete		
210	7	M-Host Lane 8 Pattern Generator LOL	Per-host lane pattern generator loss of lock flag mask	R/W Opt.
	6	M-Host Lane 7 Pattern Generator LOL		
	5	M-Host Lane 6 Pattern Generator LOL		
	4	M-Host Lane 5 Pattern Generator LOL		
	3	M-Host Lane 4 Pattern Generator LOL		
	2	M-Host Lane 3 Pattern Generator LOL		
	1	M-Host Lane 2 Pattern Generator LOL		
	0	M-Host Lane 1 Pattern Generator LOL		
211	7	M-Media Lane 8 Pattern Generator LOL	Per-media lane pattern generator loss of lock flag mask	R/W Opt.
	6	M-Media Lane 7 Pattern Generator LOL		
	5	M-Media Lane 6 Pattern Generator LOL		
	4	M-Media Lane 5 Pattern Generator LOL		
	3	M-Media Lane 4 Pattern Generator LOL		
	2	M-Media Lane 3 Pattern Generator LOL		
	1	M-Media Lane 2 Pattern Generator LOL		
	0	M-Media Lane 1 Pattern Generator LOL		
212	7	M-Host Lane 8 Pattern Checker LOL	Per-host lane pattern checker loss of lock flag mask	R/W Opt.
	6	M-Host Lane 7 Pattern Checker LOL		
	5	M-Host Lane 6 Pattern Checker LOL		
	4	M-Host Lane 5 Pattern Checker LOL		
	3	M-Host Lane 4 Pattern Checker LOL		
	2	M-Host Lane 3 Pattern Checker LOL		
	1	M-Host Lane 2 Pattern Checker LOL		
	0	M-Host Lane 1 Pattern Checker LOL		
213	7	M-Media Lane 8 Pattern Checker LOL	Latched per-media lane pattern checker loss of lock flag	R/W Opt.
	6	M-Media Lane 7 Pattern Checker LOL		

Byte	Bits	Name	Description	Type
	5	M-Media Lane 6 Pattern Checker LOL		
	4	M-Media Lane 5 Pattern Checker LOL		
	3	M-Media Lane 4 Pattern Checker LOL		
	2	M-Media Lane 3 Pattern Checker LOL		
	1	M-Media Lane 2 Pattern Checker LOL		
	0	M-Media Lane 1 Pattern Checker LOL		
214-223	7-0	Reserved		R/W

8.10.13 User Pattern

Table 8-89 provides space for the host to define a user pattern of up to 32 bytes in length. The module may not support the full 32-byte length. Refer to Table 8-75 for the maximum supported user pattern length.

Table 8-90 User Pattern (Page 13h)

Byte	Bits	Name	Description	Type
224-255	7-0	User Pattern	Host defined user pattern	RW Opt.

8.11 Page 14h (Module Diagnostics 2)

Upper memory map pages 13h and 14h are banked pages that contain module diagnostic control and status fields. The presence of Page 14h is conditional on the state of bit 5 in Page 01h byte 142 (see Table 8-28). Upper page 14h is subdivided into several areas as illustrated in the following table:

Table 8-91 Page 14h Overview

Byte	Size (bytes)	Name	Description
128	1	Diagnostics Selector	This selects the content of the data in bytes 192-255
129	1	Reserved	
130-131	2	Custom	
132-139	18	Latched Diagnostics Flags	
140-149	10	Reserved	
192-255	64	Error Information Registers	Contents defined by Diagnostics Selector

8.11.1 Diagnostics Selection Register

Byte 128 on this page selects the information being displayed in bytes 192-255. The value of this byte will revert to 0 if the selected feature is not supported. Supported features are advertised in Page 13h byte 128. Valid encodings are listed in Table 8-92. For BER measurements see Table 8-94. The values in bytes 192-255 shall be updated with the selected diagnostic data within the advertised tNACK time after byte 128 has been written.

The purpose of diagnostic selection values 01-05h is for the host to be able to read the running BER whilst gating is in progress. When gating has completed, the BER of the last gated period should be reported in bytes 192-255h when a selection value of 11h-15h is chosen. The values in bytes 192-255 shall be updated with the selected diagnostic data within the advertised tNACK time after byte 128 has been written.

The purpose of diagnostic selection values 01-05h is for the host to be able to read the running BER whilst gating is in progress. When gating has completed, the BER of the last gated period should be reported in bytes 192-255h when a selection value of 11h-15h is chosen.

Table 8-92 Diagnostics Feature Encodings

Diagnostics Selection Value	Selection	Bytes 192-255 contents
00h	None	Bytes 192-255 populated with 0's
01h	Host/Media Lane 1-8 BER	Each BER is 16 bit 11.5 floating point.
02h	Host Lane 1-4 error counters/Total Bits	
03h	Host Lane 5-8 error counters/Total Bits	
04h	Media Lane 1-4 error counters/Total Bits	
05h	Media Lane 5-8 error counters/Total Bits	
06h	Host and Media Lane 1-8 SNR and Peak Detect	
07h-10h	Reserved	
11h	Latched Host/Media Lane 1-8 BER	Each BER is 16 bit 11.5 floating point. (See Table 8-94)
12h	Latched Host Lane 1-4 error counters/Total Bits	
13h	Latched Host Lane 5-8 error counters/Total Bits	
14h	Latched Media Lane 1-4 error counters/Total Bits	
15h	Latched Media Lane 5-8 error counters/Total Bits	
16h-BFh		
C0h-FFh	Custom	

8.11.2 Latched Diagnostics Flags

The diagnostics pages include interrupt flags that are specific to diagnostics features. These interrupt flags are clear on read and behave in the same manner as non-diagnostic interrupt flags. Diagnostics interrupt flags may be masked using the mask bits in Table 8-89.

Table 8-93 Latched Diagnostics Flags (Page 14h)

Byte	Bits	Name	Description	Type
132	7	L-Loss of reference clock	Latched loss of reference clock flag for the module. Clear on Read	RO Opt.
	6-0	Reserved		
133	7-0	Reserved		RO
134	7	L-Host Lane 8 Pattern Checker Gating Complete	Latched per-host lane gating complete flag. When gating is complete, this bit will be set to 1. These bits will be cleared on read.	RO Opt.
	6	L-Host Lane 7 Pattern Checker Gating Complete		
	5	L-Host Lane 6 Pattern Checker Gating Complete		
	4	L-Host Lane 5 Pattern Checker Gating Complete		
	3	L-Host Lane 4 Pattern Checker Gating Complete		
	2	L-Host Lane 3 Pattern Checker Gating Complete		
	1	L-Host Lane 2 Pattern Checker Gating Complete		
	0	L-Host Lane 1 Pattern Checker Gating Complete		
135	7	L-Media Lane 8 Pattern Checker Gating Complete	Latched per-media lane gating complete flag. When gating is complete, this bit will be set to 1. These bits will be cleared on read.	RO Opt.
	6	L-Media Lane 7 Pattern Checker Gating Complete		
	5	L-Media Lane 6 Pattern Checker Gating Complete		
	4	L-Media Lane 5 Pattern Checker Gating Complete		
	3	L-Media Lane 4 Pattern Checker Gating Complete		
	2	L-Media Lane 3 Pattern Checker Gating Complete		
	1	L-Media Lane 2 Pattern Checker Gating Complete		
	0	L-Media Lane 1 Pattern Checker Gating Complete		
136	7	L-Host Lane 8 Pattern Generator LOL	Latched per-host lane pattern generator loss of lock flag. Clear on Read	RO Opt.
	6	L-Host Lane 7 Pattern Generator LOL		
	5	L-Host Lane 6 Pattern Generator LOL		
	4	L-Host Lane 5 Pattern Generator LOL		
	3	L-Host Lane 4 Pattern Generator LOL		
	2	L-Host Lane 3 Pattern Generator LOL		
	1	L-Host Lane 2 Pattern Generator LOL		
	0	L-Host Lane 1 Pattern Generator LOL		
137	7	L-Media Lane 8 Pattern Generator LOL	Latched per-media lane pattern generator loss of lock flag. Clear on Read	RO Opt.
	6	L-Media Lane 7 Pattern Generator LOL		
	5	L-Media Lane 6 Pattern Generator LOL		
	4	L-Media Lane 5 Pattern Generator LOL		
	3	L-Media Lane 4 Pattern Generator LOL		
	2	L-Media Lane 3 Pattern Generator LOL		
	1	L-Media Lane 2 Pattern Generator LOL		
	0	L-Media Lane 1 Pattern Generator LOL		
138	7	L-Host Lane 8 Pattern Checker LOL	Latched per-host lane pattern checker loss of lock flag. Clear on Read	RO Opt.
	6	L-Host Lane 7 Pattern Checker LOL		
	5	L-Host Lane 6 Pattern Checker LOL		
	4	L-Host Lane 5 Pattern Checker LOL		
	3	L-Host Lane 4 Pattern Checker LOL		
	2	L-Host Lane 3 Pattern Checker LOL		
	1	L-Host Lane 2 Pattern Checker LOL		
	0	L-Host Lane 1 Pattern Checker LOL		
139	7	L-Media Lane 8 Pattern Checker LOL	Latched per-media lane pattern	RO

Byte	Bits	Name	Description	Type
	6	L-Media Lane 7 Pattern Checker LOL	checker loss of lock flag. Clear on Read	Opt.
	5	L-Media Lane 6 Pattern Checker LOL		
	4	L-Media Lane 5 Pattern Checker LOL		
	3	L-Media Lane 4 Pattern Checker LOL		
	2	L-Media Lane 3 Pattern Checker LOL		
	1	L-Media Lane 2 Pattern Checker LOL		
	0	L-Media Lane 1 Pattern Checker LOL		
140-149	7-0	Reserved		RO

8.11.3 Error Information Registers

The Diagnostics Selection field in Byte 128 on this page defines what values are populated in bytes 192-255 by the module. Table 8-94 provides the details of the contents of bytes 192-255 for each defined Diagnostics Selection encoding.

Table 8-94 Bytes 192-255 Contents per Diagnostics Selector (Page 14h)

Diagnostics Selector	Bytes	Size	Lane	Bytes 192-255 contents
00h	192-255	64	Reserved	
01h	192-193	2	Host side BER, lane 1	BER in unsigned floating point 11.5 format as per SFF-8636, Error Figures section 6.7.4.4. (Big Endian), Value = m * $10^{(s-24)}$ m = mantissa s = exponent Non Zero Range is 1.000E-24 to 2.047E+10.
	194-195	2	Host side BER, lane 2	
	196-197	2	Host side BER, lane 3	
	198-199	2	Host side BER, lane 4	
	200-201	2	Host side BER, lane 5	
	202-203	2	Host side BER, lane 6	
	204-205	2	Host side BER, lane 7	
	206-207	2	Host side BER, lane 8	
	208-209	2	Media side BER, lane 1	
	210-211	2	Media side BER, lane 2	
	212-213	2	Media side BER, lane 3	
	214-215	2	Media side BER, lane 4	
	216-217	2	Media side BER, lane 5	
	218-219	2	Media side BER, lane 6	
	220-221	2	Media side BER, lane 7	
	222-211	2	Media side BER, lane 8	
02h	192-199	8	Host side error count lane 1	Little-endian format (LSB first) The total Bits 64 bit register, least significant bit, is to be used to indicate BER lock (real-time). Register 136 in Page 14h consist of the latched PRBS BER LOL. This reduces the read and
	200-207	8	Host total bits lane 1	
	208-215	8	Host side error count lane 2	
	216-223	8	Host total bits lane 2	
	224-231	8	Host side error count lane 3	
	232-239	8	Host total bits lane 3	
	240-247	8	Host side error count lane 4	

Diagnostics Selector	Bytes	Size	Lane	Bytes 192-255 contents
	248-255	8	Host total bits lane 4	the host can read a 64 byte block to measure BER. Example: An “Even” total bits means that the BER data calculated from error count bits / total bits can be trusted. An “Odd” total bits, means there is currently a BER lock problem. The BER rate will not be hardly affected by this because the total bits counter is usually very large.
03h	192-199	8	Host side error count lane 5	
	200-207	8	Host total bits lane 5	
	208-215	8	Host side error count lane 6	
	216-223	8	Host total bits lane 6	
	224-231	8	Host side error count lane 7	
	232-239	8	Host total bits lane 7	
	240-247	8	Host side error count lane 8	
	248-255	8	Host total bits lane 8	
04h	192-199	8	Media side error count lane 1	
	200-207	8	Media total bits lane 1	
	208-215	8	Media side error count lane 2	
	216-223	8	Media total bits lane 2	
	224-231	8	Media side error count lane 3	
	232-239	8	Media total bits lane 3	
	240-247	8	Media side error count lane 4	
	248-255	8	Media total bits lane 4	
05h	192-199	8	Media side error count lane 5	
	200-207	8	Media total bits lane 5	
	208-215	8	Media side error count lane 6	
	216-223	8	Media total bits lane 6	
	224-231	8	Media side error count lane 7	
	232-239	8	Media total bits lane 7	
	240-247	8	Media side error count lane 8	
	248-255	8	Media total bits lane 8	
06h	192-193	2	Host side peak detect lane 1	
	194-195	2	Host side peak detect lane 2	
	196-197	2	Host side peak detect lane 3	
	198-199	2	Host side peak detect lane 4	
	200-201	2	Host side peak detect lane 5	
	202-203	2	Host side peak detect lane 6	
	204-205	2	Host side peak detect lane 7	
	206-207	2	Host side peak detect lane 8	
	208-209	2	Host side SNR lane 1	Little-endian format (LSB first)
	210-211	2	Host side SNR lane 2	
	212-213	2	Host side SNR lane 3	
	214-215	2	Host side SNR lane 4	
	216-217	2	Host side SNR lane 5	
	218-219	2	Host side SNR lane 6	
	220-221	2	Host side SNR lane 7	

Diagnostics Selector	Bytes	Size	Lane	Bytes 192-255 contents
	222-223	2	Host side SNR lane 8	
	224-225	2	Media side peak detect lane 1	
	226-227	2	Media side peak detect lane 2	
	228-229	2	Media side peak detect lane 3	
	230-231	2	Media side peak detect lane 4	
	232-233	2	Media side peak detect lane 5	
	234-235	2	Media side peak detect lane 6	
	236-237	2	Media side peak detect lane 7	
	238-239	2	Media side peak detect lane 8	
	240-241	2	Media side SNR lane 1	Little-endian format (LSB first)
	242-243	2	Media side SNR lane 2	
	244-245	2	Media side SNR lane 3	
	246-247	2	Media side SNR lane 4	
	248-249	2	Media side SNR lane 5	
	250-251	2	Media side SNR lane 6	
	252-253	2	Media side SNR lane 7	
	254-255	2	Media side SNR lane 8	
11h	192-193	2	Latched Host side BER, lane 1	BER in unsigned floating point 11.5 format as per SFF-8636. (Big Endian), Value = m * $10^{(s-24)}$ m = mantissa s = exponent Non Zero Range is 1.000E-24 to 2.047E+10.
	194-195	2	Latched Host side BER, lane 2	
	196-197	2	Latched Host side BER, lane 3	
	198-199	2	Latched Host side BER, lane 4	
	200-201	2	Latched Host side BER, lane 5	
	202-203	2	Latched Host side BER, lane 6	
	204-205	2	Latched Host side BER, lane 7	
	206-207	2	Latched Host side BER, lane 8	
	208-209	2	Latched Media side BER, lane 1	
	210-211	2	Latched Media side BER, lane 2	
	212-213	2	Latched Media side BER, lane 3	
	214-215	2	Latched Media side BER, lane 4	
	216-217	2	Latched Media side BER, lane 5	
	218-219	2	Latched Media side BER, lane 6	
	220-221	2	Latched Media side BER, lane 7	
	222-211	2	Latched Media side BER, lane 8	
12h	192-199	8	Latched Host side error count lane 1	Little-endian format (LSB first) The total Bits 64 bit register, least significant bit, is to be used to indicate BER lock (real-time). Register 136 in Page 14h consist of the latched PRBS BER LOL. This reduces the read and the host can read a 64 byte block to measure BER.
	200-207	8	Latched Host total bits lane 1	
	208-215	8	Latched Host side error count lane 2	
	216-223	8	Latched Host total bits lane 2	
	224-231	8	Latched Host side error count lane 3	
	232-239	8	Latched Host total bits lane 3	
	240-247	8	Latched Host side error count lane 4	

Diagnostics Selector	Bytes	Size	Lane	Bytes 192-255 contents
	248-255	8	Latched Host total bits lane 4	Example: An “Even” total bits means that the BER data calculated from error count bits / total bits can be trusted. An “Odd” total bits, means there is currently a BER lock problem. The BER rate will not be hardly affected by this because the total bits counter is usually very large.
13h	192-199	8	Latched Host side error count lane 5	
	200-207	8	Latched Host total bits lane 5	
	208-215	8	Latched Host side error count lane 6	
	216-223	8	Latched Host total bits lane 6	
	224-231	8	Latched Host side error count lane 7	
	232-239	8	Latched Host total bits lane 7	
	240-247	8	Latched Host side error count lane 8	
	248-255	8	Latched Host total bits lane 8	
14h	192-199	8	Latched Media side error count lane 1	
	200-207	8	Latched Media total bits lane 1	
	208-215	8	Latched Media side error count lane 2	
	216-223	8	Latched Media total bits lane 2	
	224-231	8	Latched Media side error count lane 3	
	232-239	8	Latched Media total bits lane 3	
	240-247	8	Latched Media side error count lane 4	
	248-255	8	Latched Media total bits lane 4	
15h	192-199	8	Latched Media side error count lane 5	
	200-207	8	Latched Media total bits lane 5	
	208-215	8	Latched Media side error count lane 6	
	216-223	8	Latched Media total bits lane 6	
	224-231	8	Latched Media side error count lane 7	
	232-239	8	Latched Media total bits lane 7	
	240-247	8	Latched Media side error count lane 8	
	248-255	8	Latched Media total bits lane 8	

8.12 Pages 20h-2Fh (VDM)

Versatile diagnostics monitoring (VDM) is defined to extend the number of parameters, by up to another 256 parameters than can be monitored and alarmed per bank, in addition to the monitors and alarms already defined in Lower Memory and Pages 11h.

The Bank Register R126 can be used to extend the management memory for modules with more than 8 lanes.

Table 8-95 Summary of Page Definitions for Page 20h-2Fh

Page	Bank	Name	Description
20h	0-3	Config for Parameter 1-64 (Group 1)	Every 2-byte value defines what is being configured as VDM for the respective parameter.
21h	0-3	Config for Parameter 65-128 (Group 2)	
22h	0-3	Config for Parameter 129-192 (Group 3)	
23h	0-3	Config for Parameter 193-256 (Group 4)	
24h	0-3	Real Time Values Parameter 1-64 (Group 1)	Every 2-byte value is a read only value that returns the current value of the monitored parameter
25h	0-3	Real Time Values Parameter 65-128 (Group 2)	
26h	0-3	Real Time Values Parameter 129-192 (Group 3)	
27h	0-3	Real Time Values Parameter 193-256 (Group 4)	
28h	0-3	Threshold for Parameter 0-15 (Group 1)	Every set of 4 2-byte values is a read only threshold set
29h	0-3	Threshold for Parameter 16-31 (Group 2)	
2Ah	0-3	Threshold for Parameter 32-47 (Group 3)	
2Bh	0-3	Threshold for Parameter 48-63 (Group 4)	
2Ch	0-3	Alarms (all groups)	Every byte corresponds to 2 parameter alarms (4 bits each)
2Dh	0-3	Masks (all groups)	Every byte corresponds to 2 parameter masks (4 bits each)
2Eh	0-3	Reserved	
2Fh	0-3	Controls	

8.12.1 Pages 20h-23h (VDM Configuration Pages)

There can be up to 256 versatile parameters or monitor attributes that can be monitored. These can be either per lane, per data path or module wide parameters. Note that each page corresponds to one group.

Table 8-96 Page 20h,21h,22h,23h VDM Configuration

Page	Byte	Name	Description	Type
20h	128-129	Config VDM 1	Configuration register for VDM Parameter 1, in group 1	RO
	130-131	Config VDM 2	Configuration register for VDM Parameter 2, in group 1	RO
	132-251	Config VDM 3 to 62	Configuration registers for VDM Parameter 3 to 62, in group 1	RO
	252-253	Config VDM 63	Configuration register for VDM Parameter 63, in group 1	RO
	254-255	Config VDM 64	Configuration register for VDM Parameter 64, in group 1	RO
21h	128-129	Config VDM 65	Configuration register for VDM Parameter 65, in group 2	RO
	130-131	Config VDM 66	Configuration register for VDM Parameter 66, in group 2	RO
	132-251	Config VDM 67 to 126	Configuration registers for VDM Parameter 67 to 126, in group 2	RO
	252-253	Config VDM 127	Configuration register for VDM Parameter 127, in group 2	RO
	254-255	Config VDM 128	Configuration register for VDM Parameter 128, in group 2	RO
22h	128-129	Config VDM 129	Configuration register for VDM Parameter 129, in group 3	RO
	130-131	Config VDM 130	Configuration register for VDM Parameter 130, in group 3	RO
	132-251	Config VDM 131 to 190	Configuration registers for VDM Parameter 131 to 190, in group 3	RO
	252-253	Config VDM 191	Configuration register for VDM Parameter 191, in group 3	RO
	254-255	Config VDM 192	Configuration register for VDM Parameter 192, in group 3	RO
23h	128-129	Config VDM 193	Configuration register for VDM Parameter 193, in group 3	RO
	130-131	Config VDM 194	Configuration register for VDM Parameter 194, in group 3	RO
	132-251	Config VDM 195 to 254	Configuration registers for VDM Parameter 195 to 254, in group 3	RO
	252-253	Config VDM 255	Configuration register for VDM Parameter 255, in group 3	RO
	254-255	Config VDM 256	Configuration register for VDM Parameter 256, in group 3	RO

8.12.1.1 Versatile VDM Configuration Setting Bytes

Each Diagnostics can be specified by a two-byte configuration parameter.

Table 8-97 Definition of 2-byte Configuration parameter

Byte	Bits	Description
MSB (Even)	7-4	Threshold ID. This number corresponds to which threshold set will be used for this parameter. The Threshold is defined to be in the same group as the parameter configuration. Page 20h: (group 1) Threshold ID = 1 + value of this field. Page 21h: (group 2): Threshold ID = 17 + value of this field Page 22h: (group 3): Threshold ID = 33 + value of this field Page 23h: (group 4): Threshold ID = 49 + value of this field
	3-0	0: Lane 1 or data path starting on lane 1 1: Lane 2 or data path on lane 2 2: Lane 3 or data path on lane 3 3: Lane 4 or single-host-lane data path on lane 4 4: Lane 5 or single-host-lane data path on lane 5 5: Lane 6 or single-host-lane data path on lane 6 6: Lane 7 or single-host-lane data path on lane 7 7: Lane 8 or single-host-lane data path on lane 8 15: Module
LSB (Odd)		Parameter type (see Table 8-99)

8.12.1.2 Versatile VDM Configuration Parameter List

The table below defines the list of parameters. All parameters are 16-bit values. Each 16-bit value may be either

- Unsigned (U16)
- Signed (S16)
- Unsigned 16-bit floating point (F16; BER floating point format).

Unsigned 16-bit floating point numbers use 5 bits for base-10 exponent, offset by -24, and 11 bits for mantissa. The format is:

$m*10s+o$

Where m ranges from 0 to 2047 (11 bits), s ranges from 0 to 31 (5 bits) and o is fixed at -24. The smallest non-zero number is m=1 and s=0 or 1*10^(-24). The largest number supported is m=2047 and s=31, or 2.047*10^10. Within the 2 bytes of the value (stored lowest byte first), m and s are encoded as follows:

Table 8-98 Encoding for BER/FERC

Byte	Bits	Description
1	7:3	Exponent (s)
1	2:0	Mantissa (m), bits 10:8
2	7:0	Mantissa (m), bits 7:0

Table 8-99 Definition of 2-byte Configuration parameter (Type Coding)

Type Value	Description	Data Type	LSB Scaling	Unit
0	Parameter not supported[1]	N/A		
1	Laser Age (0% at BOL, 100% EOL)	U16	1	%
2	TEC Current	S16	100/32767	%
3	Laser Frequency Error	S16	10	MHz
4	Laser Temperature	S16	1/256	C
5	eSNR Media Input	U16	1/256	dB
6	eSNR Host Input	U16	1/256	dB
7	PAM4 Level Transition Parameter (LTP) Media Input	U16	1/256	dB
8	PAM4 Level Transition Parameter (LTP) Host Input	U16	1/256	dB
9	Pre-FEC BER Minimum Media Input (data-path)	F16	N/A	
10	Pre-FEC BER Minimum Host Input.	F16	N/A	
11	Pre-FEC BER Maximum Media Input.	F16	N/A	
12	Pre-FEC BER Maximum Host Input.	F16	N/A	
13	Pre-FEC BER Average Media Input.	F16	N/A	
14	Pre-FEC BER Average Host Input.	F16	N/A	
15	Pre-FEC BER Current Value Media Input.	F16	N/A	
16	Pre-FEC BER Current Value Host Input.	F16	N/A	
17	Errored Frames Minimum Media Input	F16	N/A	
18	Errored Frames Minimum Host Input	F16	N/A	
19	Errored Frames Maximum Media Input	F16	N/A	
20	Errored Frames Minimum Host Input	F16	N/A	
21	Errored Frames Average Media Input	F16	N/A	
22	Errored Frames Average Host Input	F16	N/A	
23	Errored Frames Current Value Media Input	F16	N/A	
24	Errored Frames Current Value Host Input	F16	N/A	
25-99	Reserved			
100-127	Custom Parameter			
128-255	Reserved for Coherent			

[1] This value means that the module is not presenting any data on the corresponding real-time value, or latched flag registers.

8.12.2 Pages 24h-27h (VDM Real Time Value Pages)

There are 256 real time values. These are read only monitors that has been configured per configuration settings in pages 20h-23h.

Table 8-100 Page 24h-27h Real-Time Monitored Parameter Values

Page	Byte	Name	Description	Type
24h	128-129	Real-time VDM 1	Real-time value of VDM Parameter 1, in group 1, MSB in lower address.	RO
	130-131	Real-time VDM 2	Real-time value for VDM Parameter 2, in group 1, MSB in lower address.	RO
	132-251	Real-time VDM 3 to 62	Real-time values for VDM Parameter 3 to 62, in group 1, MSB in lower address.	RO
	252-253	Real-time VDM 63	Real-time value for VDM Parameter 63, in group 1, MSB in lower address.	RO
	254-255	Real-time VDM 64	Real-time value for VDM Parameter 64, in group 1, MSB in lower address.	RO
25h	128-129	Real-time VDM 65	Real-time value of VDM Parameter 65, in group 2, MSB in lower address.	RO
	130-131	Real-time VDM 66	Real-time value for VDM Parameter 66, in group 2, MSB in lower address.	RO
	132-251	Real-time VDM 67 to 126	Real-time values for VDM Parameter 67 to 126, in group 2, MSB in lower address.	RO
	252-253	Real-time VDM 127	Real-time value for VDM Parameter 127, in group 2, MSB in lower address.	RO
	254-255	Real-time VDM 128	Real-time value for VDM Parameter 128, in group 2, MSB in lower address.	RO
26h	128-129	Real-time VDM 129	Real-time value of VDM Parameter 129, in group 3, MSB in lower address.	RO
	130-131	Real-time VDM 130	Real-time value for VDM Parameter 130, in group 3, MSB in lower address.	RO
	132-251	Real-time VDM 131 to 190	Real-time values for VDM Parameter 131 to 190, in group 3, MSB in lower address.	RO
	252-253	Real-time VDM 191	Real-time value for VDM Parameter 191, in group 3, MSB in lower address.	RO
	254-255	Real-time VDM 192	Real-time value for VDM Parameter 192, in group 3, MSB in lower address.	RO
27h	128-129	Real-time VDM 193	Real-time value of VDM Parameter 193, in group 4, MSB in lower address.	RO
	130-131	Real-time VDM 194	Real-time value for VDM Parameter 194, in group 4, MSB in lower address.	RO
	132-251	Real-time VDM 195 to 254	Real-time values for VDM Parameter 195 to 254, in group 4, MSB in lower address.	RO
	252-253	Real-time VDM 255	Real-time value for VDM Parameter 255, in group 4, MSB in lower address.	RO
	254-255	Real-time VDM 256	Real-time value for VDM Parameter 256, in group 4, MSB in lower address.	RO

8.12.3 Pages 28h-2Bh (VDM Threshold Pages)

Table 8-101 Page 28h-2Bh Alarm/Warning Thresholds

Page	Byte	Name	Description	Type
28h	128-129	Threshold ID 0 High Alarm	Thresholds for group 1 monitored parameters. Each threshold is MSB first, and in the same units as the real-time value.	RO
	130-131	Threshold ID 0 Low Alarm		RO
	132-133	Threshold ID 0 High Warning		RO
	134-135	Threshold ID 0 Low Warning		RO
	136-137	Threshold ID 1 High Alarm		RO
	138-139	Threshold ID 1 Low Alarm		RO
	140-141	Threshold ID 1 High Warning		RO
	142-143	Threshold ID 1 Low Warning		RO
		...		RO
	248-249	Threshold ID 15 High Alarm		RO
	250-251	Threshold ID 15 Low Alarm		RO
	252-253	Threshold ID 15 High Warning		RO
	254-255	Threshold ID 15 Low Warning		RO
29h	128-129	Threshold ID 16 High Alarm	Thresholds for group 2 monitored parameters. Each threshold is MSB first, and in the same units as the real-time value.	RO
	130-131	Threshold ID 16 Low Alarm		RO
	132-133	Threshold ID 16 High Warning		RO
	134-135	Threshold ID 16 Low Warning		RO
	136-137	Threshold ID 17 High Alarm		RO
	138-139	Threshold ID 17 Low Alarm		RO
	140-141	Threshold ID 17 High Warning		RO
	142-143	Threshold ID 17 Low Warning		RO
		...		RO
	248-249	Threshold ID 31 High Alarm		RO
	250-251	Threshold ID 31 Low Alarm		RO
	252-253	Threshold ID 31 High Warning		RO
	254-255	Threshold ID 31 Low Warning		RO
2Ah	128-129	Threshold ID 32 High Alarm	Thresholds for group 3 monitored parameters. Each threshold is MSB first, and in the same units as the real-time value.	RO
	130-131	Threshold ID 32 Low Alarm		RO
	132-133	Threshold ID 32 High Warning		RO

	134-135	Threshold ID 32 Low Warning		RO
	136-137	Threshold ID 33 High Alarm		RO
	138-139	Threshold ID 33 Low Alarm		RO
	140-141	Threshold ID 33 High Warning		RO
	142-143	Threshold ID 33 Low Warning		RO
		...		RO
	248-249	Threshold ID 47 High Alarm		RO
	250-251	Threshold ID 47 Low Alarm		RO
	252-253	Threshold ID 47 High Warning		RO
	254-255	Threshold ID 47 Low Warning		RO
2Bh	128-129	Threshold ID 48 High Alarm	Thresholds for group 4 monitored parameters. Each threshold is MSB first, and in the same units as the real-time value.	RO
	130-131	Threshold ID 48 Low Alarm		RO
	132-133	Threshold ID 48 High Warning		RO
	134-135	Threshold ID 48 Low Warning		RO
	136-137	Threshold ID 49 High Alarm		RO
	138-139	Threshold ID 49 Low Alarm		RO
	140-141	Threshold ID 49 High Warning		RO
	142-143	Threshold ID 49 Low Warning		RO
		...		RO
	248-249	Threshold ID 63 High Alarm		RO
	250-251	Threshold ID 63 Low Alarm		RO

8.12.4 Page 2Ch (VDM Alarms)

Each VDM parameter can raise alarms and warnings. Page 2Ch consists of the alarm and warnings of configured alarms. Each set of alarm consist of 4 bits. All the alarm bits are latched, set to active logic 1 when an alarm is raised and then "Cleared On Read" COR if the TWI read occurs and the alarm is no longer present.

Table 8-102 Alarm Bit

Byte	Bit	Name	Description
Any	0 or 4	High Alarm Bit	If alarm exceed high alarm threshold this bit will be raised.
	1 or 5	Low Alarm Bit	If alarm exceed low alarm threshold this bit will be raised.
	2 or 6	High Warning Bit	If alarm exceed high warning threshold this bit will be raised.
	3 or 7	Low Warning Bit	If alarm exceed low warning threshold this bit will be raised.

Table 8-103 Page 2Ch Alarm and Warning Configuration

Byte	Bit	Name	Description	Type
128	7-4	L-Alarms for VDM 2	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #2, in group 1	RO/COR
	3-0	L-Alarms for VDM 1	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #1, in group 1	RO/COR
129-158	7-0	L-Alarms for VDM 3-62	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #3-62, in group 1	RO/COR
159	7-4	L-Alarms for VDM 64	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #64, in group 1	RO/COR
	3-0	L-Alarms for VDM 63	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #63, in group 1	RO/COR
160	7-4	L-Alarms for VDM 66	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #66, in group 2	RO/COR
	3-0	L-Alarms for VDM 65	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #65, in group 2	RO/COR
161-190	7-0	L-Alarms for VDM 67-126	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #67-126, in group 1	RO/COR
191	7-4	L-Alarms for VDM 128	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #128, in group 2	RO/COR
	3-0	L-Alarms for VDM 127	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #127, in group 2	RO/COR
192	7-4	L-Alarms for VDM 130	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #130, in group 3	RO/COR
	3-0	L-Alarms for VDM 129	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #129, in group 3	RO/COR
193-222	7-0	L-Alarms for VDM 131-190	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #131-190, in group 1	RO/COR
223	7-4	L-Alarms for VDM 192	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #192, in group 3	RO/COR
	3-0	L-Alarms for VDM 191	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #191, in group 3	RO/COR
224	7-4	L-Alarms for VDM 194	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #194, in group 4	RO/COR
	3-0	L-Alarms for VDM 193	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #193, in group 4	RO/COR
224-254	7-0	L-Alarms for VDM 195-254	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #195-254, in group 1	RO/COR
255	7-4	L-Alarms for VDM 256	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #256, in group 4	RO/COR
	3-0	L-Alarms for VDM 255	High, Low Alarm and Warning Latches, defined in Table 8-104, for parameter #255, in group 4	RO/COR

8.12.5 Page 2Dh (VDM Mask)

Each VDM parameter can raise an alarm or warning flag as described in Page 2Ch. Each asserted flag shall also assert the Interrupt signal if the flag has not been masked out. Page 2Dh defines a writeable page of alarm mask bits for the corresponding alarm bit defined in Page 2Ch.

Table 8-104 Page 2Dh Threshold ID 0 to 15 Alarm and Warning Configuration

Byte	Bit	Name	Description	Type
128	7-4	M-Flags for VDM 2	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #2, in group 1	RW
	3-0	M-Flags for VDM 1	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #1, in group 1	RW
129-158	7-0	M-Flags for VDM 3-62	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #3-62, in group 1	RW
159	7-4	M-Flags for VDM 64	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #64, in group 1	RW
	3-0	M-Flags for VDM 63	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #63, in group 1	RW
160	7-4	M-Flags for VDM 66	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #66, in group 2	RW
	3-0	M-Flags for VDM 65	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #65, in group 2	RW
161-190	7-0	M-Flags for VDM 67-126	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #67-126, in group 1	RW
191	7-4	M-Flags for VDM 128	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #128, in group 2	RW
	3-0	M-Flags for VDM 127	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #127, in group 2	RW
192	7-4	M-Flags for VDM 130	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #130, in group 3	RW
	3-0	M-Flags for VDM 129	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #129, in group 3	RW
193-222	7-0	M-Flags for VDM 131-190	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #131-190, in group 1	RW
223	7-4	M-Flags for VDM 192	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #192, in group 3	RW
	3-0	M-Flags for VDM 191	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #191, in group 3	RW
224	7-4	M-Flags for VDM 194	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #194, in group 4	RW
	3-0	M-Flags for VDM 193	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #193, in group 4	RW
224-254	7-0	M-Flags for VDM 195-254	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #195-254, in group 1	RW
255	7-4	M-Flags for VDM 256	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #256, in group 4	RW
	3-0	M-Flags for VDM 255	High, Low Alarm and Warning Masks, defined in Table 8-104, for parameter #255, in group 4	RW

8.12.6 Page 2Fh (VDM Advertisement and Controls)

Page 2Fh is used for advertisement and controls of the Versatile Diagnostics Monitoring features. Byte 128 advertises which pages 20h-2Bh, and which parts of pages 2Ch and 2Dh are supported.

Byte 144, bit 7 is used to request that the counters that are listed as Minimum, Maximum, or Average values be latched by the module. Setting and clearing this bit can be considered as a Performance Monitoring Interval.
The process for Performance Monitoring Intervals is as follows:

1. If not already clear, host clears Latch Request to 0
2. Module (within tNACK) clears Latch Clear Done to 0
3. Module copies internally latched data to real-time reporting registers
4. Module sets Latch Clear Done to 1
5. Host may read real-time reporting registers to get in-interval data. The module is directly updating real-time reporting data.
6. Host sets Latch Request to 1, requesting to end the interval and start a new one (atomically)
7. Module (within tNACK) clears Latch Done to 0
8. Module stops updating real-time reporting registers, resets internal latches and then continues to update internally latched data without copying to real-time reporting registers
9. Module sets Latch Done to 1
10. Host is now free to read the (non-changing) real-time reporting registers to gather the data from the interval that just ended. The module is updating internal registers, but not reporting data.
11. Host may clear Latch Request to 0 either immediately after reading prior interval data, or just prior to ending the new interval.

See the BER/FERC section 9.3.7 below for details on the reporting register values in relationship to the Latch Requests.

Table 8-105 Versatile VDM Page 2Fh Control Registers Summary

Byte	Bit	Name	Description	Type
128	7-2	Reserved		RO
	1-0	Versatile VDM Page support	0: Group 1 (Page 20h, 24h, 28h, first ¼ of 2Ch, 2Dh) 1: Groups 1,2 (Page 20h-21h, 24h-25h, 28h-29h, first ½ of 2Ch, 2Dh) 2: Groups 1-3 (Page 20h-22h, 24h-26h, 28h-2Ah, first ¾ of 2Ch, 2Dh) 3: Groups 1-4 (Page 20h-23h, 24h-27h, 28h-2Bh, 2Ch, 2Dh)	RO
129-130	7-0	Fine Interval Length	Length of fine interval used for internal BER/FERC monitoring. 16-bit signed, MSB first, with LSB = 0.1 ms	RO
131-143	7-0	Reserved		RO
144	7	Latch Request	When set to 1 by the host, causes the module to latch and hold all reported minimum, maximum and average values. When set to 0 by the host, release the latch request, allowing the reported minimum, maximum and average values to update. Note that the module must record new data even while this counter is latched so that no data is lost.	RW
	6-0	Reserved		RO
145	7	Latch Done	Set to 0 by the module within tNACK time from when Latch Request is set to 1 by the host. Set to 1 by the module when it has finished latching and restarting all supported counters.	RO
	6	Latch Clear Done	Set to 0 by the module within tNACK time from when Latch Request is set to 0 by the host. Set to 1 by the module when it has finished releasing the latches and begun real-time updates of the data.	RO
	5-0	Reserved		RO
146-255	7-0	Reserved		RO

8.12.7 VDM Detailed Description of Monitored Parameters

8.13 Page 9Fh (CDB Messaging)

Page 9Fh contains the command and local payload fields for the optional Command Data Block (CDB) feature. See section 7.2 for CDB usage. Implementation of page 9Fh is dependent on the CDB Implemented field in Table 8-35.

Bytes 128-135 contain fields for the host to specify the CDB command to be executed by the module, the length of the payload for write operations, and a checksum for these bytes. Bytes 136-255 contain the local payload (LPL), for payloads of 120 bytes or less. These fields are described in detail in Table 8-106.

Table 8-106 Page 9Fh fields

Byte	Bits	Name	Description	Type
128	7-0	CDB Command MSB	CDB command code to be executed by the module, see Table 10-8 for a list of command codes. A host write to CDB Command LSB triggers the module to execute the command. The host must write the length, checksum, payload (if applicable), and CDB Command MSB prior to writing the CDB Command LSB byte. If the host writes a new CDB command before the current CDB command completes without first checking the STS_BUSY bit the behavior is unpredictable.	RW RQD.
129	7-0	CDB Command LSB		
130	7-0	EPL Length MSB	Length of the Extended Payload (EPL) that will be written to pages A0h-AFh, in bytes. Valid lengths are 0-2048.	RW Opt.
131	7-0	EPL Length LSB		
132	7-0	LPL Length	Length of the Local Payload (LPL) that will be written to bytes 136-255 on this page, in bytes. The LPL Length is used to calculate the CdbChkCode field.	RW Opt.
133	7-0	CdbChkCode	CdbChkCode is the one's complement of the summation of page 9Fh Bytes 128 to (135+LPL_Length) with Bytes 133,134 and 135 equal to 0.	RW RQD.
134	7-0	RLPLLen Response LPL Length	Response LPL Length is an encoded value that describes the length of the data returned by the specified CDB command code. This byte should be written to 0 when sending commands. RLPLLen = 0. RLPLChkCode = 0. This is set by the module upon completion of the CDB command if the response message does not consist of any data. RLPLLen = 0. RLPLChkCode = FFh. This is set by the module for CDB messages that returns a payload but the module does not support the calculation of RLPLChkCode for this command. RLPLLen = 0. RLPLChkCode = 01h to FEh. This should not be returned by the module. RLPLLen =1 to 120. This is set by the module to indicate that the CDB response length is indicated by RLPLLen. RLPLChkCode is the one's complement of the summation of the response message which is Byte/s 136 to (RLPLLen - 1).	RW Opt.

Byte	Bits	Name	Description	Type
			RLPLLen = 121 to 239. Reserved. RLPLChkCode should be set to 0. RLPLLen = 240 to 255 (F0h to FFh) These encodings are used to return the RLPLChkCode for EPL pages A0h to AFh. Here RLPLChkCode is the one's complement of the summation of all bytes in the page (128 to 255) of page/s A0h to ((RLPLLen – F0h) + A0h). Here the RLPLChkCode only calculates the data of all bytes within the EPL page/s, all unused or undefined bytes will be calculated assuming these bytes are 00h. The module may set these unused bytes to 00h on the return payload data.	
135	7-0	RLPLChkCode Response LPL ChkCode	Response LPL ChkCode is a CDB CMD Code dependent. See description from Byte 134 RLPLLen above. This byte should be written to 0 when sending commands.	RW Opt.
136-255	7-0	Local Payload (LPL)	Local Payload data of size N, where Nmax=120. Local Payload contains either host-written data or module-written data, depending on the CDB Command.	RW Opt.

A CDB command is triggered when byte 129 is written. The module may process the CDB command at the end of the TWI transaction or at the time that byte 129 is written. Hence, the recommended method for the host to invoke a CDB command is to issue a minimum of two TWI transactions:

- Step 1: Write bytes 130 to (135+LPL Len). These writes may have to be broken into multiple TWI transactions, based on the CDB Max TWI Bytes Per Write Transaction advertisement in Table 8-35 or based on host capabilities.
- Step 2: Write the 16-bit CDB command using one of two methods
    - Method 1: Write bytes 128 and 129 in a single TWI transaction
    - Method 2: Write byte 128 in one TWI transaction, followed by a write to byte 129 in a second TWI transaction

The host shall not write bytes 128 to (135+LPL Len) in one TWI transaction, as the outcome is unpredictable.

Either the EPL Length field or LPL Length field is populated by the host if the associated CDB Command requires a host-written payload. If the CDB Command requires the module to write the payload, the length of the payload is embedded in the payload. Host implementers should note that both the EPL Length and LPL Length fields are included in the Checksum even when they are not used, so it is recommended that host implementers write a 0 to unused fields. Writing a 0 to LPL Length allows the host to avoid zeroing the LPL Payload block. See the CDB Command definition in section 9 for a per-command definition of whether EPL or LPL should be used.

The Checksum in byte 133 protects only the contents of page 9Fh, including the CDB command, EPL and LPL length, and the entire LPL block (as defined by LPL length). If an EPL checksum or check code is required, a command specific checksum should be defined for each CMD code that uses EPL data in commands.

The time when a CDB command processing starts depends on the bit value in Page 01h Byte 165 Bit 7. Assuming that the current page is 9Fh, CDB processing is triggered in either of the two following cases:

- a TWI write data to Byte 129 is received by the module (Page01h Byte165 Bit7=0b)
- a TWI stop bit is received within a TWI write data transaction that includes Bytes 129 (Page 01h Byte165 Bit7=1b)

In the first method, a minimum of two TWI transactions shall be required to invoke a CDB command. In the

second method a single TWI transaction is sufficient to invoke a CDB command. The choice between these two methods depends on the module vendor. The host shall control the module as defined by the module vendors' advertisement of the control bit. Note that the maximum number of bytes per TWI transaction for CDB is advertised in Page 01h Byte 164.

In either method, the LPL Length field and/or the EPL Length field is populated by the host and is CDB command dependent. A command may be defined to use either LPL or EPL or both LPL and EPL. Host implementers should note that both the LPL Length and EPL Length fields are included in the CdbCheckCode and it is recommended that host implementers write 0's to these fields when a command does not use any LPL or EPL.

Commands using LPL shall populate the LPL before the CDB command is triggered. In these type of commands the CdbCheckCode in byte 133 shall be calculated by the host and sent together with the command. This protects the content of page 9Fh, including the CDB command, LPL length, EPL length and the entire LPL block as defined by the LPL length.

Commands using EPL shall populate the EPL before the CDB command is triggered. For commands using EPL, The length of the EPL and any additional command EPL check codes to ensure validity of EPL data are not defined here. If these additional check codes are required, they are to be specified independently for each type or group of command codes. For example, firmware load assumes that the CDB data written in the EPL block comes directly from the user provided file read as a binary stream and it is up to the user to add any additional check codes to any data embedded within the file.

8.13.1 Triggering CDB on Writes to Page 9Fh Byte 129

If the module advertises that a CDB command is triggered by a write to Byte 129, then the recommended method for the host to invoke a CDB command consist of a minimum of two TWI transactions:

- Step 1. Write bytes 130 to (135+LPL Len). These writes may have to be broken into multiple TWI transactions based on the CDB Max TWI Bytes Per Write Transaction advertisement in Page 01h Byte 164 as well as the host capabilities. NOTE: RLPLLen and RLPLChkCode should be written to 0.
- Step 2. Write the 16-bit CDB command using one of the two methods.
    - Method 1: Write bytes 128 and 129 in a single TWI transaction.
    - Method 2: Write byte 128 in one TWI transaction followed by a write to byte 129 in a second TWI transaction.

The host shall not write bytes 128 to (135+LPL Len) in one TWI transaction, as the outcome will be unpredictable.

8.13.2 Triggering CDB on STOP bit

If the module advertises that a CDB command is triggered by a stop bit, the TWI (sequential) write transaction shall include Byte 129, otherwise the CDB command will not be invoked. Here the recommended method for the host to invoke a CDB command consist of a minimum of one TWI transaction. The maximum bytes per TWI transaction shall not exceed what the module advertises in Page 01h Byte 164.

- Write bytes 128 to (135+LPL Len) in one TWI transaction. Although Byte 129 is sent on the 2nd byte the command is not processed until the STOP bit is received.

If the maximum bytes per TWI transaction is 8, then commands with LPL Len of 0 can only be invoked with a single TWI transaction. If the maximum bytes per TWI transaction is 128, then any CDB commands that uses LPL only may be triggered in one CDB transaction by sending an TWI sequential write from Bytes 128 to (135+LPL Len).

The host may still use multiple TWI transactions or byte by byte transactions, as a single byte write to Byte 129 will also invoke a CDB command. (A single byte write includes Byte 129 and a STOP bit).

8.14 Pages A0h-AFh (CDB Extended Payload Pages)

Pages A0-AFh contain the Extended Payload (EPL) for the optional Command Data Block (CDB) feature. See section 7.2 for CDB usage. Implementation of pages A0h-AFh is dependent on the CDB Implemented field and the Number of EPL Pages Implemented field, both in Table 8-35.

If the CDB Auto Paging Implemented bit is set to 1 (see Table 8-35), host reads or writes past the end of pages A0h-AEh cause the module to automatically increment the page number and wrap the address pointer to the beginning of the next page (byte 128). If CDB Auto Paging Implemented bit is set to 0, host reads or writes past the end of pages will wrap around to the Byte 128 of the same page as described in section 5.4.1 and section 5.4.4.1 respectively.

Table 8-107 Page A0H-AFh fields

Byte	Bits	Name	Description	Type
128-255	7-0	Extended Payload (EPL)	Extended Payload data of size N, where Nmax=2048. Extended Payload contains either host-written data or module-written data, depending on the CDB Command.	RW Opt.

9 CDB Command Reference

9.1 CDB Command Group Summary

CDB is an optional feature. If CDB is implemented then some commands within each CDB command groups may be required. The "Type" column in Table 9-1 defines if the CDB group is "Required" or "Optional". Within each group there will be a similar "Type" column indicating if the specific command is required or optional.

Table 9-1 CDB Command Code Groups

Code Range		Group	Description	Group Type	Sec
from	to				
0000h	003Fh	Module Commands	CDB module level commands.	Req	9.2
0040h	005Fh	Command Advertisement	Advertises the features of the CDB block.	Req	9.3
0060h	006Fh	Bulk Read Commands	Use CDB to manage bulk read of banks and pages.	Opt	9.4
0070h	007Fh	Bulk Write Commands	Use CDB to manage bulk write of banks and pages.	Opt	9.5
0080h	00FFh	Reserved			
0100h	011Fh	Firmware Download	Firmware Download using CMIS	Opt	9.6
0120h	01FFh	Reserved			
0200h	027Fh	Performance Monitoring	Performance Monitoring Data.	Opt	9.7
0280h	02FFh	Data Recording Monitoring	Data Recording and Monitoring, where data is to be stored in the module as non volatile data.	Opt	9.8
0300h	03FFh	BERT		Opt	9.9
0380h	03FFh	Diagnostics		Opt	9.10
0400h	3FFFh	Reserved			
4000h	7FFFh	Reserved for OIF	Reserved for OIF. Coherent applications under OIF may also use the reserved sections within the groups itself. This section simply reserves this CMD group for OIF to define new groups of messages specific for the application.		
8000h	FFFFh	Reserved for Vendor Use	Reserved for Vendor Use		

9.2 CDB Module Commands

Table 9-2 CDB Module Commands Summary

CMD Code	Name	Description	Type	Section
0000h	QUERY - Status	QUERY. The module returns a CDB status of success (01h) as well as some basic status information of the module, such as password unlock status. This can also be used to check if CDB is implemented.	Req	10.2.1
0001h	Enter Password	The module password that is traditionally entered in Bytes 122-125 may be entered using this CDB command. Entering password using CDB allows the module to indicate the error codes especially if the password is rejected. Currently entering password using Bytes 122-125 does not have feedback if the password is accepted or rejected.	Opt	10.2.2
0002h	Change Password	In the current module, changing the password persistently is defined by writing to Bytes 118-121, which do not have a feedback to the user if the operation completed successfully. This command allows for the module to indicate if the new password has been properly and successfully stored in non-volatile memory or if there were any errors during the operation to change the module password.	Opt	10.2.3
0003h	Enable/Disable Password Protection	Disable password protection for writing to the user EEPROM	Opt	10.2.4
0004h	Abort Current Background Operation	Abort Current Background Operation	Opt	
0005h-001Fh	Reserved			

9.2.1 CMD 0000h: QUERY Status

This QUERY command may be used to return the module password acceptance status and to perform a test on the CDB interface. The delay time parameter in the message defines a host specified delay before the module is to return with the response and asserts the CDB complete flag. This can be used as a test especially if the module advertises Page 01 Byte 163 bit 5 that CDB operates in the background or not. If the TWI is enabled during this time, CDB status should return "In Progress" status until the delay time has expired. If TWI is disabled, then the TWI will NACK until the delay time has elapsed and the CDB response is ready.

The return message shows the current module unlock level. It also shows that even if CDB for firmware download is implemented, the firmware download feature may still be locked until a specific special password is available from the module vendor. This is to prevent accidental erasures of various areas of firmware.

Table 9-3 CDB Command 0000h: QUERY-Status

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Query command code used to extract status of CDB.	0000h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	02h
9Fh	133	CdbChkCode	Bytes 128 to 137 calculated with Bytes 133-135=0	
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136	Delay time MSB	Programmable delay time in ms for this command to respond. If 0 respond immediately as fast as the module can process the message.	
9Fh	137	Delay time LSB		
CDB flags and status field				
00h	8	CDB complete flag	This command assert the CDB complete flag.	
00h	37 or 38	CDB Status	**In Progress** 10 000001b=Busy capturing command 10 000010b=Busy checking/validating command 10 000011b=Busy executing command **On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000101b=CdbChkCode error	
Module return LPL				
9Fh	136	Length of Status	Length of this message including this byte	3
9Fh	137	Unlock level and privileges	0000 0000b=Module Boot Up. 0000 0001b=Password Accepted. 1xxx xxxxb = Vendor password accepted. Other bits indicate internal vendor information. Vendor passwords are passwords with Bit 31 set in the password field.	
9Fh	138	Firmware download allowed.	00h Firmware download feature is locked 01h Firmware download feature is unlocked. To unlock firmware download either the standard or MSA password may be used. (module dependent)	

Page	Byte	Name	Description	Value
9Fh	139-255	Not returned		

9.2.2 CMD 0001h: Enter Password

Table 9-4 CDB Command 0001h: Enter Password

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Enter Password command code. Different passwords may be implemented by different module vendors.	0001h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	04h
9Fh	133	CdbChkCode	Bytes 128 to 139 calculated with Bytes 133-135=0	
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136-139	Password		
CDB flags and status fields				
00h	8	CDB complete flag	This command does not assert the CDB complete flag and will NACK until command is completed.	
00h	37 or 38	CDB Status	**On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000101b=CdbChkCode error 01 000110b=Password error – not accepted	
Module return LPL				
9Fh	136-255	No return payload		

9.2.3 CMD 0002h: Change Password

Table 9-5 CDB Command 0002h: Change Password

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Change Password. Only MSA-level password can be changed.	0002h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	04h
9Fh	133	CdbChkCode	Bytes 128 to 139 calculated with Bytes 133-135=0	
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136-139	New password		

Page	Byte	Name	Description	Value
CDB flags and status fields				
00h	8	CDB complete flag	This command does not assert the CDB complete flag and will NACK until the command is complete. Since a non volatile memory is to be written this command may take up to 80 msec.	
00h	37 or 38	CDB Status	**On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error (e.g. Bit 31 is set). 01 000101b=CdbChkCode error 01 000110b=Insufficient privilege to change password	
Module return LPL				
9Fh	136-255	No return payload		

9.2.4 CMD 0003h: Enable/Disable Password Protection

Table 9-6 CDB Command 0003h: Enable/Disable Password Protection

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Features enabled or disabled when password Byte 122-125 is entered and accepted.	0003h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	01h
9Fh	133	CdbChkCode	Bytes 128 to 136 calculated with Bytes 133-135=0	
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136	Disable Protection	D0: 0b. Password protection for writing Pg 3 Enabled. 1b. Password protection for writing Pg 3 Disabled.	
CDB flags and status fields				
00h	8	CDB complete flag	This command does not assert the CDB complete flag and will NACK until the command is complete.	
00h	37 or 38	CDB Status	**On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000101b=CdbChkCode error	
Module return LPL				
9Fh	136-255	No return payload		

9.2.5 CMD 0004h: General ABORT

Table 9-7 CDB Command 0004h: Abort

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Abort the current background operation. This operation is used to abort a CDB command.	0004h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	00h
9Fh	133	CdbChkCode	Bytes 128 to 139 calculated with Bytes 133-135=0	FCh
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136-255	Reserved		
CDB flags and status fields				
00h	8	CDB complete flag	This command does not assert the CDB complete flag and will NACK until the command is complete.	
00h	37 or 38	CDB Status	**On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000101b=CdbChkCode error 01 000110b=Insufficient privilege to change password	
Module return LPL				
9Fh	136-255	No return payload		

9.3 CDB Feature and Capabilities Implemented

Table 9-8 CDB Feature and Capabilities Commands Overview

CMD Code	Name	Description	Type	Section
0040h	Module Features	Identify which commands are supported. CMD Codes 0000h to 00FFh.	Req	10.3.1
0041h	Firmware Update features	Identify all features that firmware update features support. CMD Codes 0100h to 011Fh.	Req	10.3.2
0042h	Performance Monitoring	Method and FW download commands that are supported	Req	10.3.3
0042h-005Fh	Reserved			

9.3.1 CMD 0040h: Module Features Implemented

Table 9-9 CDB Command 0040h: Module Features Implemented

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Advertises module feature CMDs implemented.	0040h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	00h
9Fh	133	CdbChkCode	Bytes 128 to 135 calculated with Bytes 133-135=0	BFh
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136-255	Reserved		
CDB flags and status fields				
00h	8	CDB complete flag	This command does not assert the CDB complete flag and will NACK until command is completed.	
00h	37 or 38	CDB Status	On Success 00 000001b=Success, no specific message On Failure 01 000000b=Failed, no specific failure code 01 000101b=CdbChkCode error	
Module return LPL				
9Fh	136	CDB flags	Reserved for additional CDB flags.	00h
9Fh	137	Reserved		00h
9Fh	138	CMDs 0000h-0007h support	Each bit represent a mask. If bit is “1” then command is implemented D0: CMD 0000h is implemented. .. D7: CMD 0007h is implemented.	
9Fh	139	CMDs 0008h-000Fh		
9Fh	140	CMDs 0010h-0017h		
9Fh	141	CMDs 0018h-001Fh		
9Fh	142	CMDs 0020h-0027h		
9Fh	143	CMDs 0028h-002Fh		
9Fh	144	CMDs 0030h-0037h		
9Fh	145	CMDs 0038h-003Fh		
9Fh	146	CMDs 0040h-0047h		
9Fh	147	CMDs 0048h-004Fh		
9Fh	148	CMDs 0050h-0057h		
9Fh	149	CMDs 0058h-005Fh		
9Fh	150	CMDs 0060h-0067h	Bulk Read commands implemented flags.	
9Fh	151	CMDs 0068h-006Fh	Bulk Read commands implemented flags.	
9Fh	152	CMDs 0070h-0077h	Bulk Write commands implemented flags.	
9Fh	153	CMDs 0078h-007Fh	Bulk Write commands implemented flags.	
9Fh	154-169	CMDs 0080h-00FFh		
9Fh	170	Max CDB Cmd Time (MSB) ms	Maximum CDB command execution time. If time exceeds this value the host may send the CDB Abort Command. Maximum time per CDB command is 65.535 seconds.	
9Fh	171	Max CDB Cmd Time (LSB) ms		
9Fh	172-255	Not returned		

9.3.2 CMD 0041h: Firmware Update Features Implemented

Table 9-10 CDB Command 0041h: Firmware Update Features Implemented

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Advertises firmware update features CMDs implemented.	0041h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	00h
9Fh	133	CdbChkCode	Bytes 128 to 135 calculated with Bytes 133-135=0	BEh
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136-255	Reserved		
CDB flags and status fields				
00h	8	CDB complete flag	This command does not assert the CDB complete flag and will NACK until command is completed.	
00h	37 or 38	CDB Status	On Success 00 000001b=Success, no specific message On Failure 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b= CdbChkCode error 01 000110b=Insufficient privilege to change password	
Module return LPL				
9Fh	136	Firmware download password type	00h: Download unlocked by vendor password 01h: Download unlocked by vendor password sequence 80h: Download unlocked by standard MSA password	
9Fh	137	Copy, Abort, Full Image Readback	Bit0: 0b. Abort 0102h Not Supported. 1b. Abort 0102h Supported. Bit1: 0b. Copy 0108h Not Supported. 1b. Copy 0108h Supported. Bit2: 0b. Skipping erased blocks Not Supported. 1b. Skipping erased blocks Supported. Bit3-6: Reserved Bit7: 0b. Full Image Readback Not Supported. 1b. Full Image Readback Supported. (See section 7.2.2)	
9Fh	138	Start command payload size	This defines the number of bytes in the start command that must be extracted from the binary file and sent to the module.	
9Fh	139	Erased Byte	This is the default erased byte. Typically for NAND flash erased state is FFh or some flash or EEPROM technology it is 00h. The purpose of this byte is such that the wire transfer time may be optimized	

Page	Byte	Name	Description	Value
9Fh	140	bsize	Maximum firmware download block size for optimum firmware upgrade performance. This byte defines the maximum block size to write or read data, encoded as Block size = (bsize + 1) * 8 E.g. bsize = 0. Block Size = 8. E.g. bsize = 13. Block Size = 112. E.g. bsize = 63. Block Size = 512. E.g. bsize = 255. Block Size = 2048. NOTE: Pg01 Byte 164 indicates the maximum TWI interface for the whole CDB block. The block size advertised by the module explicitly indicates the maximum size of the Write LPL or EPL block for the firmware download feature.	
9Fh	141	Write LPL / EPL	Firmware upgrade supported mechanism. 00h : None Supported. 01h : Write to LPL supported. 10h : Write to EPL supported. 11h : Both Write to LPL and EPL supported.	
9Fh	142	Read LPL / EPL	Firmware read / readback support mechanism. 00h : None Supported. 01h : Read to LPL supported. 10h : Read to EPL supported. 11h : Both Write to LPL and EPL supported.	
9Fh	143	Run Image A or B hitless supported.	0 : CMD Run A or B causes a reset. Traffic is affected. 1 : CMD Run A or B may reset but module will do its best to maintain traffic and management states. Data path functions are not reset.	
9Fh	144	CMD Start 0101h max time ms (MSB)	This is the maximum execution time for a CDB Start command to complete execution.	
9Fh	145	CMD Start 0101h max time ms (LSB)		
9Fh	146	CMD Abort 0102h max time ms (MSB)	This is the maximum execution time for a CDB Abort command to complete execution.	
9Fh	147	CMD Abort 0102h max time ms (LSB)		
9Fh	148	CMD Write 0103h/ 0104h max time ms (MSB)	This is the maximum execution time for a CDB Write command to complete execution.	
9Fh	149	CMD Write 0103h/ 0104h max time ms (LSB)		
9Fh	150	CMD Complete 0107h max time ms (MSB)	This is the maximum execution time for a CDB Complete command to complete execution.	
9Fh	151	CMD Complete 0107h max time ms (LSB)		
9Fh	152	CMD Copy 0108h max time ms (MSB)	This is the maximum execution time for a CDB Copy command to complete execution.	
9Fh	153	CMD Copy 0108h max time ms (LSB)		
9Fh	154-255	Not Returned		

9.3.3 CMD 0042h: Performance and Data Monitoring Features Implemented

Table 9-11 CDB Command 0042h: Performance and Data Monitoring Features Implemented

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Advertises performance and data monitoring features CMDs implemented.	0042h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	00h
9Fh	133	CdbChkCode	Bytes 128 to 135 calculated with Bytes 133-135=0	BDh
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136-255	Reserved		
CDB flags and status fields				
00h	8	CDB complete flag	This command does not assert the CDB complete flag and will NACK until command is completed.	
00h	37 or 38	CDB Status	**On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000101b=CdbChkCode error	
Module return LPL				
9Fh	136	CMDs 0200h-0207h support	Each bit represent a mask. If bit is “1” then command is implemented D0: CMD 0200h is implemented. .. D7: CMD 0207h is implemented.	
9Fh	137	CMDs 0208h-020Fh	Each bit represent a mask. If bit is “1” then command is implemented D0: CMD 0208h is implemented. .. D7: CMD 020Fh is implemented.	
9Fh	138-151	CMDs 0210h-027Fh	Bitmask defines command implemented.	
9Fh	152	CMDs 0280h-0287h	Data Monitoring Command Implemented. D0: CMD 0280h implemented. .. D7: CMD 0287h is implemented.	
9Fh	153-167	CMDs 0288h-02FFh		
9Fh	168-255	Not returned		

9.3.4 CMD 0043h: BERT and Diagnostics Features Implemented

Table 9-12 CDB Command 0043h: BERT and Diagnostics Features Implemented

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Advertises performance and data monitoring features CMDs implemented.	0043h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	00h
9Fh	133	CdbChkCode	Bytes 128 to 135 calculated with Bytes 133-135=0	BCh
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136-255	Reserved		
CDB flags and status fields				
00h	8	CDB complete flag	This command does not assert the CDB complete flag and will NACK until command is completed.	
00h	37 or 38	CDB Status	**On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000101b=CdbChkCode error	
Module return LPL				
9Fh	136	CMDs 0300h-0307h support	Each bit represent a mask. If bit is “1” then command is implemented D0: CMD 0300h is implemented. .. D7: CMD 0307h is implemented.	
9Fh	137	CMDs 0308h-030Fh	Each bit represent a mask. If bit is “1” then command is implemented D0: CMD 0308h is implemented. .. D7: CMD 030Fh is implemented.	
9Fh	138-151	CMDs 0310h-037Fh	Bitmask defines command implemented.	
9Fh	152	CMDs 0380h-0387h	Data Monitoring Command Implemented. D0: CMD 0380h implemented. .. D7: CMD 0387h is implemented.	
9Fh	153-167	CMDs 0388h-03FFh		
9Fh	168-255	Not returned		

9.4 CDB Bulk Read Commands

Table 9-13 CDB Bulk Read Commands Overview

CMD Code	Name	Description	Type	Section
0060h-006Fh	Reserved			

9.5 CDB Bulk Write Commands

Table 9-14 CDB Bulk Write Commands Overview

CMD Code	Name	Description	Type	Section
0070h-007Fh	Reserved			

9.6 CDB Firmware Download Commands

Firmware download using CDB is an optional feature.

Table 9-15 CDB Firmware Download Commands Overview

CMD Code	Name	Description	Type	Section
0100h	Get firmware Info	When the host issues this command, the module returns the requested FW information of all field-updateable firmwares in the module.	Req	10.6.1
0101h	Start firmware download	The host issues this command to initiate a firmware update. The module may completely erase the target or simply acknowledge and prepare the module firmware for any appropriate update or dynamically erase as each data blocks arrives. On success, the host may begin sending the firmware image using command code 0102h-0107h.	Opt	10.6.2
0102h	Abort firmware download	Aborts the FW Download if a FW Start has been issued.	Opt	10.6.3
0103h	Write firmware Image using LPL	After issuing this command, the host may begin writing the firmware image in the LPL page. The module transfers the new firmware image into non-volatile storage. The firmware image transfer from the host to module is covered by the CDB command block checksum, but this checksum does not ensure that the image has been properly transferred to non-volatile storage.	Opt	10.6.4
0104h	Write firmware Image using EPL	After issuing this command, the host may begin writing the firmware image in the EPL page(s). The module transfers the new firmware image into non-volatile storage. The firmware image transfer from the host to module is covered by a block checksum, but this checksum does not ensure that the image has been properly transferred to non-volatile storage.	Opt	10.6.5
0105h	Read firmware Image using LPL	The host may use this command to read back the firmware image that was most recently written to non-volatile storage. The module copies the image from non-volatile storage to the LPL page. The firmware image transfer from the module to the host is covered by the CDB command block checksum, but this checksum does not ensure that the image has been properly transferred from non-volatile storage to the LPL page.	Opt	10.6.6
0106h	Read firmware Image using EPL	The host may use this command to read back the firmware image that was most recently written to non-volatile storage. The module copies the image from non-volatile storage to the EPL page(s). The firmware image transfer from the module to host is covered by a block checksum, but this checksum does not ensure that the image has been properly transferred from non-volatile storage to the EPL page(s).	Opt	10.6.7

CMD Code	Name	Description	Type	Section
0107h	Complete firmware download.	The host issues this command when the entire firmware image has been written into the LPL or EPL pages. If this command is not issued, the firmware cannot be run even if the image is properly loaded to non-volatile storage. The module validates the checksum associated with the image when the host issues this command.	Opt	10.6.8
0108h	Copy firmware image	For architectures where multiple images are supported for a given subsystem in the module, this command causes the module to copy an image from one non-volatile storage location to another one. It is assumed that the copy firmware image command includes a validation process by the module firmware to ensure the copied image is valid. This is so that the CDB complete firmware image command 0107h does not need to be called after a copy firmware image command.	Opt	10.6.9
0109h	Run firmware image	This command is used to switch between running images for architectures where multiple images are supported for a given subsystem in the module. If the running image number is the same as the image number in this command, this command has no effect. If the module supports hitless update, this command is used to transfer control to the new firmware.	Opt	10.6.10
010Ah	Commit firmware image	The host uses this command to Commit the running image so that the module will boot from it on future boots. The assumption is that the host has a time period where it runs the new firmware and “accepts” the new firmware. During this time, if a reset occurs, the previously committed image will be run. When the host issues this command, the module will mark a non-volatile storage location to be used after future module resets. Only the running image can be committed. This is to avoid committing a “bad” image.	Opt	10.6.11
010Bh-011Fh	Reserved			

9.6.1 CMD 0100h: Get Firmware Info

Table 9-16 CDB Command 0100h: Get firmware Info

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	This command returns the firmware versions and firmware default running images that resides in the module. Firmware images A, B and either a factory or boot firmware image version.	0100h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	00h
9Fh	133	CdbChkCode	Bytes 128 to 135 calculated with Bytes 133-135=0	FEh
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136-255	No host-written payload		
CDB flags and status fields				
00h	8	CDB complete flag	This command does not assert the CDB complete flag and will NACK until the command is completed.	
00h	37 or 38	CDB Status	**On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b=CdbChkCode error 01 000110b=Password error – insufficient privilege	
Module return LPL				
9Fh	136	Firmware Status Flags	Bitmask to indicate FW Status. 00h: Factory Boot Image is running (if Factory Image is supported) Bit 0: Image A is running Bit 1: Image A is committed, module boots from Image A Bit 2: Image A is erased/empty Bit 3: Reserved Bit 4: Image B is running Bit 5: Image B is committed, module boots from Image B Bit 6: Image B is erased/empty Bit 7: Reserved	
9Fh	137	Information block	Bit 0: Firmware image A is present in the fields below. Bit 1: Firmware image B is present in the fields below. Bit 2: Factory or Boot image is present in the fields below.	
9Fh	138	Image A Major	Image A firmware major revision	
9Fh	139	Image A Minor	Image A firmware minor revision	
9Fh	140-141	Image A Build	Image A firmware build number	
9Fh	142-173	Image A Extra String		
9Fh	174	Image B Major	Image B firmware major revision	
9Fh	175	Image B Minor	Image B firmware minor revision	
9Fh	176-177	Image B Build	Image B firmware build number	

Page	Byte	Name	Description	Value
9Fh	178-209	Image B Extra String		
9Fh	210	Factory or Boot Major	Factory or Boot image firmware major revision	
9Fh	211	Factory or Boot Minor	Factory or Boot image firmware minor revision	
9Fh	212-213	Factory or Boot Build	Factory or Boot image firmware build number	
9Fh	214-245	Factory or Boot Extra String		
9Fh	246-255	Not Returned		

9.6.2 CMD 0101h: Start Firmware Download

Table 9-17 CDB Command 0101h: Start Firmware Download

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Start the firmware download process. The module may erase the whole image or simply prepare for the firmware to be updated. The duration of this command depends on the host-written payload of the command. A complete erase of an image may take several seconds.	0101h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	LPL Len
9Fh	133	CdbChkCode	Bytes 128 to (135+LPLlen) calculated with Bytes 133-135=0	
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136-139	Image Size	Size of firmware image to download into the module. This should be the file size including the LPL Len bytes sent as vendor data in this message.	
9Fh	140-143	Reserved		0h
9Fh	144-255	Vendor Data	The vendor may send up to 112 bytes of information in the START firmware download command. It is recommended that the binary file delivered has up to 112 bytes of header that is sent to the module. This information within this field can be used by a vendor to reject an incorrect file (binary file) and prevent firmware loading of the incorrect file presented to the module.	
CDB flags and status fields				
00h	8	CDB complete flag	CDB complete flag is set when command has completed.	
00h	37 or 38	CDB Status	**In Progress** 10 000001b=Busy processing command, CMD captured 10 000010b=Busy processing command, CMD checking 10 000011b=Busy processing command, CMD execution **On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b=CdbChkCode error 01 000110b=Password error – insufficient privilege	
Module return LPL				
9Fh	136-255	Payload	Return message contains an empty payload. Contents unspecified	

9.6.3 CMD 0102h: Abort Firmware Download

Table 9-18 CDB Command 0102h: Abort Firmware Download

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Abort the firmware update process. Modules supporting only a single image should not implement this command and advertise accordingly.	0102h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	00h
9Fh	133	CdbChkCode	Bytes 128 to 135 calculated with Bytes 133-135=0	
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136-255	No host-written payload		
CDB flags and status fields				
00h	8	CDB complete flag	CDB complete flag is set when command has completed.	
00h	37 or 38	CDB Status	**In Progress** 10 000001b=Busy processing command, CMD captured 10 000010b=Busy processing command, CMD checking 10 000011b=Busy processing command, CMD execution **On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b=CdbChkCode error 01 000110b=Password error – insufficient privilege	
Module return LPL				
9Fh	136-255	Payload	Return message contains an empty payload. Contents unspecified	

9.6.4 CMD 0103h: Write Firmware Image LPL

Table 9-19 CDB Command 0103h: Write Firmware Image LPL

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Write one block of the firmware image into the LPL	0103h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	LPL Len
9Fh	133	CdbChkCode	Bytes 128 to (135+LPL Len) calculated with Bytes 133-135=0	
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136-139	addr – block address	Starting byte address of this block of data within the supplied image file minus the size of the size of the "Start Command Payload Size". See section 7.2.2.1.	
9Fh	140-255	Firmware image	One block of the firmware image. Byte 134 defines the length of this data block	
CDB flags and status fields				
00h	8	CDB complete flag	CDB complete flag is set when command has completed.	
00h	37 or 38	CDB Status	**In Progress** 10 000001b=Busy processing command, CMD captured 10 000010b=Busy processing command, CMD checking 10 000011b=Busy processing command, CMD execution **On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b= CdbChkCode error 01 000110b=Password error – insufficient privilege	
Module return LPL				
9Fh	136-255	No module return payload		

9.6.5 CMD 0104h: Write Firmware Image EPL

Table 9-20 CDB Command 0104h: Write Firmware Image EPL

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Write one block of the firmware image into the EPL	0104h
9Fh	130-131	EPL Len	Length of EPL for this command.	XXXX
9Fh	132	LPL Len	Length of LPL for this command.	04h
9Fh	133	CdbChkCode	Bytes 128 to 139 calculated with Bytes 133-135=0	
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136-139	addr – block address	Starting byte address of this block of data within the supplied image file minus the size of the size of the "Start Command Payload Size". See section 7.2.2.1.	
9Fh	140-255	Reserved		
Host-written EPL				
A0h-AFh	128-255	Firmware image		
CDB flags and status fields				
00h	8	CDB complete flag	CDB complete flag is set when command has completed.	
00h	37 or 38	CDB Status	**In Progress** 10 000001b=Busy processing command, CMD captured 10 000010b=Busy processing command, CMD checking 10 000011b=Busy processing command, CMD execution **On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b=CdbChkCode error 01 000110b=Password error – insufficient privilege	
Module return LPL				
9Fh	136-255	Payload	Return message contains an empty payload. Contents unspecified	
Module return EPL				
A0h-AFh	128-255	Reserved		

9.6.6 CMD 0105h: Read Firmware Image LPL

Table 9-21 CDB Command 0105h: Read Firmware Image LPL

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Read firmware image from the indicated block in non-volatile storage into the LPL	0105h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	06h
9Fh	133	CdbChkCode	Bytes 128 to 141 calculated with Bytes 133-135=0	
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136-139	addr – block address	Starting byte address of this block of data within the supplied image file minus the size of the size of the "Start Command Payload Size". See section 7.2.2.1.	
9Fh	140	Length MSB	Number of bytes to read back to the LPL in this command, starting at the indicated address.	
9Fh	141	Length LSB		
9Fh	142-255	Reserved		
CDB flags and status fields				
00h	8	CDB complete flag	CDB complete flag is set when command has completed.	
00h	37 or 38	CDB Status	**In Progress** 10 000001b=Busy processing command, CMD captured 10 000010b=Busy processing command, CMD checking 10 000011b=Busy processing command, CMD execution **On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b=CdbChkCode error 01 000110b=Password error – insufficient privilege	
Module return LPL				
9Fh	136-139	Address of block	Base address of the data block within the firmware image	
9Fh	140-255	Image		

9.6.7 CMD 0106h: Read Firmware Image EPL

Table 9-22 CDB Command 0106h: Read Firmware Image EPL

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Read firmware image from the indicated block in non-volatile storage into the EPL	0106h
9Fh	130-131	EPL Len	Length of EPL for this command.	XXXX
9Fh	132	LPL Len	Length of LPL for this command.	06h
9Fh	133	CdbChkCode	Bytes 128 to 141 calculated with Bytes 133-135=0	
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136-139	addr – block address	Starting byte address of this block of data within the supplied image file minus the size of the size of the "Start Command Payload Size". See section 7.2.2.1.	
9Fh	140	Length MSB	Number of bytes to read back to the EPL in this command, starting at the indicated address.	
9Fh	141	Length LSB		
9Fh	142-255	Reserved		
Host-written EPL				
A0h-AFh	128-255	Reserved		
CDB flags and status fields				
00h	8	CDB complete flag	CDB complete flag is set when command has completed.	
00h	37 or 38	CDB Status	**In Progress** 10 000001b=Busy processing command, CMD captured 10 000010b=Busy processing command, CMD checking 10 000011b=Busy processing command, CMD execution **On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b=CdbChkCode error 01 000110b=Password error – insufficient privilege	
Module return LPL				
9Fh	136-255	Payload	Return message contains an empty payload. Contents unspecified	
Module return EPL				
A0h-AFh	128-255	Image		

9.6.8 CMD 0107h: Firmware Download Complete

Table 9-23 CDB Command 0107h: Firmware Download Complete

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	When the host issues this command, the module shall validate the complete image and then return success or failure (could be checksum failure)	0107h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	00h
9Fh	133	CdbChkCode	Bytes 128 to 135 calculated with Bytes 133-135=0	F7h
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136-255	No host-written payload		
CDB flags and status fields				
00h	8	CDB complete flag	CDB complete flag is set when command has completed.	
00h	37 or 38	CDB Status	**In Progress** 10 000001b=Busy processing command, CMD captured 10 000010b=Busy processing command, CMD checking 10 000011b=Busy processing command, CMD execution **On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b=CdbChkCode error 01 000110b=Password error – insufficient privilege	
Module return LPL				
9Fh	136-255	No module return payload		

9.6.9 CMD 0108h: Copy Firmware Image

Copy Image is an optional command within the firmware download commands that may be used in the firmware update process. This command is typically used in a system where both images that are written to flash are identical, and thus if the host desires to have both images A and B be identical, it can simply tell the module to copy from the "active, committed" running image to the "inactive, uncommitted" backup image.

Table 9-24 CDB Command 0108h: Copy Firmware Image

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Optional Copy Firmware Image command	0108h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	01h
9Fh	133	CdbChkCode	Bytes 128 to 136 calculated with Bytes 133-135=0	
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136	Copy Direction	ABh: Copy Image A into Image B BAh: Copy Image B into Image A	
9Fh	137-255	Reserved		
CDB flags and status fields				
00h	8	CDB complete flag	CDB complete flag is set when command has completed.	
00h	37 or 38	CDB Status	**In Progress** 10 000001b=Busy processing command, CMD captured 10 000010b=Busy processing command, CMD checking 10 000011b=Busy processing command, CMD execution **On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b=CdbChkCode error 01 000110b=Password error – insufficient privilege	
Module return LPL				
9Fh	136-139	Length	Number of bytes copied	
9Fh	140	Copy Direction	ABh: Image A was copied into Image B BAh: Image B was copied into Image A	
9Fh	141	Status of Copy	00h : No Error in copy 01h : Copy Failed	
9Fh	142-255	Reserved		

9.6.10 CMD 0109h: Run Image

After firmware has been updated, this command is used to tell the module to switch to the new firmware version. The host may use CMD 0100h to determine both the active and inactive firmware versions.

Executing the Run Image command may potentially be hitless, non-disruptive or minimally disruptive to high-speed traffic. Behavior of the module and its control loop transients during resets are vendor and technology dependent if this feature is being supported by the module as advertised.

Table 9-25 CDB Command 0109h: Run FW Image

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	The host uses this command to run the inactive image.	0109h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	00h
9Fh	133	CdbChkCode	Bytes 128 to 138 calculated with Bytes 133-135=0	F4h
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136	Reserved		
9Fh	137	Reset Mode	00h: Running the inactive image is not hitless and may include a full reset. 01h: Attempt a hitless restart to the inactive image.	
9Fh	138	Delay to Reset ms (MSB)	Indicate the number of ms after receiving this command before a reset will occur starting from the time the CDB complete flag is set. (or NACK clearing if the CDB background mode is not set). A delay time of 0 will mean that the module will reset immediately upon success and then host may not be able to have time to read the CDB status message.	
9Fh	139	Delay to Reset ms (LSB)		
9Fh	139-255	Reserved		
CDB flags and status fields				
00h	8	CDB complete flag	CDB complete flag is set when command has completed.	
00h	37 or 38	CDB Status	**In Progress** 10 000001b=Busy processing command, CMD captured 10 000010b=Busy processing command, CMD checking 10 000011b=Busy processing command, CMD execution **On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b=CdbChkCode error 01 000110b=Password error – insufficient privilege	
Module return LPL				
9Fh	136-255	Payload	Return message contains an empty payload. Contents unspecified	

9.6.11 CMD 010Ah: Commit Image

A Commit is the process where the “running” image is set to be the image to be used on exit from module reset. In other words, a committed image is the image that will run and is expected to be a 'good' firmware version to run upon any resets (including watch dog).

This command is used to switch the committed image after the firmware update process, when the new firmware is running and when the host has determined that the new firmware is working properly. The module shall only execute a Commit Image command on the image that it is currently running. If a non-running image is allowed to be committed, it is possible that a bad version may be committed and attempted to run after the next module reset.

Table 9-26 CDB Command 010Ah: Commit Image

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code		010Ah
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	00h
9Fh	133	CdbChkCode	Bytes 128 to 136 calculated with Bytes 133-135=0	F4h
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136-255	Reserved		
CDB flags and status fields				
00h	8	CDB complete flag	CDB complete flag is set when command has completed.	
00h	37 or 38	CDB Status	**In Progress** 10 000001b=Busy processing command, CMD captured 10 000010b=Busy processing command, CMD checking 10 000011b=Busy processing command, CMD execution **On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b=CdbChkCode error 01 000110b=Password error – insufficient privilege	
Module return LPL				
9Fh	136-255	Reserved	Return message contains an empty payload. Contents unspecified	

9.7 CDB Performance Monitoring

Table 9-27 CDB Performance Monitoring Commands Overview

CMD Code	Name	Description	Type	Section
0200h	PM Controls	General Performance Monitoring Controls	Req	10.7.1
0201h	PM Feature Advertisement	Additional Advertisement on which PM is supported.	Req	10.7.2
0202h-020Fh	Reserved			
0210h	PM Module Params LPL	Module-level PM using LPL only	O	10.7.3
0211h	PM Module Params EPL	Module-level PM using EPL only	O	10.7.3
0212h	PM Host Side Per Lane LPL	Lane-specific host side PM using LPL only	O	10.7.4
0213h	PM Host Side Per Lane EPL	Lane-specific host side PM using EPL only	O	10.7.4
0214h	PM Media Side Per Lane LPL	Lane-specific media side PM using LPL only	O	10.7.5
0215h	PM Media Side Per Lane EPL	Lane-specific media side PM using EPL only	O	
0216h	PM Data Path LPL	Lane-specific data path PM using LPL only	O	10.7.6
0217h	PM Data Path EPL	Lane-specific data path PM using EPL only	O	
0209h-027Fh	Reserved			

9.7.1 CMD 0200h: PM Controls

This section details the messages used to extract PM data records such as minimum, average, maximum values. Unless otherwise specified, a 2 byte or 4 byte value is encoded in Big Endian format i.e. the lowest byte address consist of the most significant byte of the word.

Table 9-28 CDB Command 0200h: PM Controls

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Controls the behavior of the Performance Monitoring block and its behavior with respect to the Versatile Diagnostic Monitoring in Page 20h-2Fh.	0200h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	04h
9Fh	133	CdbChkCode	Bytes 128 to 139 calculated with Bytes 133-135=0	
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136	Mode	Bit 0: PM Objects Synchronous to Page 20h-2Fh. 0b: PM Objects are Independent. 1b: PM Objects are the same as 20h-2Fh (linked). When PM objects are linked, this means that data in page 20-2Fh shares the same objects as the data in the CDB block. It also means that clearing the latch using either method in Pg 2Fh will clear the latches in the CDB block. Bit 1-7 Reserved. Set to 0.	
9Fh	137	Reserved		00h
9Fh	138	Clear All Latches all Lanes	Bit 0 0b: No operation. This command used to change other control attributes. 1b: Clear all minimum, average, maximum latches for all managed parameters for all lanes at the same time as best as possible. Bit 1-7 Reserved. Set to 0.	
9Fh	139	Reserved		00h
9Fh	140-255	Reserved	Not sent	
CDB flags and status fields				
00h	8	CDB complete flag	This command does not assert the CDB complete flag and will NACK until command is completed.	
00h	37 or 38	CDB Status	**On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b=CdbChkCode error 01 000110b=Password error – insufficient privilege	

Page	Byte	Name	Description	Value
Module return LPL				
9Fh	136-255	Reserved.		

9.7.2 CMD 0201h: PM Additional Feature Advertisement.

Table 9-29 CDB Command 0201h: PM Feature Advertisement

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Identifies which of the PM monitors defined in CMD 0210h to 0217h is supported by the module.	0201h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	04h
9Fh	133	CdbChkCode	Bytes 128 to 139 calculated with Bytes 133-135=0	
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136	Host Side Monitor	Bit0: Host Side SNR monitor available. Bit1: Host Side LTP monitor available.	
9Fh	137	Media Side Monitor	Line Side SNR monitor available. Line Side LTP monitor available.	
9Fh	138	Reserved		00h
9Fh	139	Reserved		00h
9Fh	140-255	Reserved	Not sent	
CDB flags and status fields				
00h	8	CDB complete flag	This command does not assert the CDB complete flag and will NACK until command is completed.	
00h	37 or 38	CDB Status	**On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b=CdbChkCode error 01 000110b=Password error – insufficient privilege	
Module return LPL				
9Fh	136-255	Reserved.		

9.7.3 CMD 0210h/0211h: Module PM using LPL/EPL

Table 9-30 CDB Command 0210h/0211h: Module PM using LPL/EPL

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Return Module PM using LPL.	0210h
			Return Module PM using EPL.	0211h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	05h
9Fh	133	CdbChkCode	Bytes 128 to 140 calculated with Bytes 133-135=0	
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136	Clear latch Mode	Bit 0: 0b: PM Object consists of 6 bytes (minimum, average and maximum) 1b: PM object consists of 8 bytes and includes a “current” value. Bit 1-5: Reserved Bit 7: 0b: return the PM data 1b: return the selected PM data and then reset the latching of the selected PM data.	
9Fh	137	Selected PM data	Bit 0: Module Temperature Bit 1: Vcc Bit 2: Aux1 Bit 3: Aux2 Bit 4: Aux3 Bit 5-7: Reserved	
9Fh	138	Reserved	Reserved	
9Fh	139	Reserved Coherent	Reserved for Coherent	
9Fh	140	Vendor	Reserved for Vendor	
9Fh	141-255	Reserved		
CDB flags and status fields				
00h	8	CDB complete flag	CDB complete flag is set when command has completed.	
00h	37 or 38	CDB Status	**In Progress** 10 000001b=Busy processing command, CMD captured 10 000010b=Busy processing command, CMD checking 10 000011b=Busy processing command, CMD execution **On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b=CdbChkCode error 01 000110b=Password error – insufficient privilege	

Page	Byte	Name	Description	Value
Returned Module PM Data using LPL (CMD 0210h)				
9Fh	136-255	LPL PM data (up to 120 bytes)	Module PM object of one PM parameter consists of 6 to 8 bytes. 2 bytes – minimum value 2 bytes – average (mean) value 2 bytes – maximum value 2 bytes – an optional current value A maximum of 15 to 20 objects can be returned using LPL depending on if the optional current value is present. The first PM object data is the first bit set starting from Bytes 137-140 of this 0210h command.	
Returned Module PM Data using EPL (CMD 0211h)				
A0h to AFh	128-255	EPL PM data (number of bytes depends on available pages)	Module PM object of one PM parameter consists of 6 to 8 bytes. 2 bytes – minimum value 2 bytes – average (mean) value 2 bytes – maximum value 2 bytes – an optional current value The maximum number of objects depends on the size of the EPL and the optional current value present bit value. If multiple A0h-AFh pages are present then the data is expected to be contiguous across pages. The first PM object data is the first bit set starting from Bytes 137-140 of this 0211h command.	

9.7.4 CMD 0212h/0213h: PM Host Side Per-Lane LPL/EPL

Table 9-31 CDB Command 0212h/0213h: PM Host Side Per-Lane LPL

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Host Side Per Lane PM using LPL	0212h
			Host Side Per Lane PM using EPL	0213h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	14h
9Fh	133	CdbChkCode	Bytes 128 to 155 calculated with Bytes 133-135=0	
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136	Clear latch Mode	Bit 0: 0b: PM Object consists of 6 bytes (minimum, average and maximum) 1b: PM object consists of 8 bytes and includes a “current” value. Bit 1-5: Reserved Bit 7: 0b: return the PM data 1b: return the selected PM data and then reset the latching of the selected PM data.	
9Fh	137-139	Reserved	In future, we could define start/stop/increment lanes here if needed for modules with more than 32 lanes.	
9Fh	140	Bitmask Lane 32-25	Bitmask indicating which lane is present. These encoding allow for Bytes 140-143 to be interpreted as a 32 bit Big Endian word, where bit 0 represents lane 1 and bit 31 represent lane 32.	
9Fh	141	Bitmask Lane 24-17		
9Fh	142	Bitmask Lane 16-9		
9Fh	143	Bitmask Lane 8-1		
9Fh	144	Selected PM data	Bit 0: Host Side Lane SNR Bit 1: Host Side PAM4 LTP Bit 2: Host Side PreFEC BER Bits 3-7 : Reserved	
9Fh	145-147	Selected PM data	Reserved	
9Fh	148-151	Selected PM data	Reserved for Coherent.	
9Fh	152-155	Selected PM data	Reserved for Vendor.	
CDB flags and status fields				
00h	8	CDB complete flag	CDB complete flag is set when command has completed.	
00h	37 or 38	CDB Status	**In Progress** 10 000001b=Busy processing command, CMD captured 10 000010b=Busy processing command, CMD checking 10 000011b=Busy processing command, CMD execution **On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b= CdbChkCode error 01 000110b=Password error – insufficient privilege	

Page	Byte	Name	Description	Value
Returned Host Side Per Lane PM Using LPL (0212h)				
9Fh	136-255	LPL PM data (up to 120 bytes)	Module PM object of one PM parameter consists of 6 to 8 bytes. 2 bytes – minimum value 2 bytes – average (mean) value 2 bytes – maximum value 2 bytes – an optional current value A maximum of 15 to 20 objects can be returned using LPL depending if the optional current value is present. The first PM object data is from the lowest set bit in the lane bitmask of the first bit set starting from Bytes 144-155 of this 0212h command.	
Returned Host Side Per Lane PM Using EPL (0213h)				
A0h to AFh	128-255	EPL PM data (number of bytes depends on available pages)	Module PM object of one PM parameter consists of 6 to 8 bytes. 2 bytes – minimum value 2 bytes – average (mean) value 2 bytes – maximum value 2 bytes – an optional current value The maximum number of objects depends on the size of the EPL and the optional current value present bit value. If multiple A0h-AFh pages are present then the data is expected to be contiguous across pages. The first PM object data is from the lowest bit set to 1b in the lane bitmask. i.e. the first bit set to 1b starting from Bytes 144-155 of this 0213h command.	

9.7.5 CMD 0214h/0215h: PM Media Side Per-Lane LPL/EPL

Table 9-32 CDB Command 0214h/0215h: PM Media Side Per-Lane LPL/EPL

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Media Side Per Lane PM using LPL	0214h
			Media Side Per Lane PM using EPL	0215h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	14h
9Fh	133	CdbChkCode	Bytes 128 to 155 calculated with Bytes 133-135=0	
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136	Clear latch Mode	Bit 0: 0b: PM Object consists of 6 bytes (minimum, average and maximum) 1b: PM object consists of 8 bytes and includes a “current” value. Bit 1-5: Reserved Bit 7: 0b: return the PM data 1b: return the selected PM data and then reset the latching of the selected PM data.	
9Fh	137-139	Reserved	Reserved for modules with more than 32 lanes.	
9Fh	140	Bitmask Lane 32-25	Bitmask indicating which lane is present. This encoding allows for Bytes 140-143 to be interpreted as a 32 bit Big Endian word, (bit 0 represents lane 1 and bit 31 represent lane 32).	
9Fh	141	Bitmask Lane 24-17		
9Fh	142	Bitmask Lane 16-9		
9Fh	143	Bitmask Lane 8-1		
9Fh	144	Selected PM data	Bit 0: Media Side SNR Bit 1: Media Side PAM4 LTP Bits 2-7 : Reserved	
9Fh	145	Selected PM data	Bit 0: Tx Bias Bit 1: Tx Power Bit 2: Rx Power Bit 3: Per-Lane Laser Temperature Bits 4-7 : Reserved	
9Fh	146-147	Selected PM data	Reserved	
9Fh	148-151	Selected PM data	Reserved for Coherent.	
9Fh	152-155	Selected PM data	Reserved for Vendor.	

Page	Byte	Name	Description	Value
CDB flags and status fields				
00h	8	CDB complete flag	CDB complete flag is set when command has completed.	
00h	37 or 38	CDB Status	**In Progress** 10 000001b=Busy processing command, CMD captured 10 000010b=Busy processing command, CMD checking 10 000011b=Busy processing command, CMD execution **On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b= CdbChkCode error 01 000110b=Password error – insufficient privilege	
Returned Media Side Per Lane PM Using LPL (0214h)				
9Fh	136-255	LPL PM data (up to 120 bytes)	Module PM object of one PM parameter consists of 6 to 8 bytes. 2 bytes – minimum value 2 bytes – average (mean) value 2 bytes – maximum value 2 bytes – an optional current value A maximum of 15 to 20 objects can be returned using LPL depending if the optional current value is present. The first PM object data is from the lowest bit set to 1b in the lane bitmask. i.e. the first bit set to 1b starting from Bytes 144-155 of this 0214h command.	
Returned Media Side Per Lane PM Using EPL (0215h)				
A0h to AFh	128-255	EPL PM data (number of bytes depends on available pages)	Module PM object of one PM parameter consists of 6 to 8 bytes. 2 bytes – minimum value 2 bytes – average (mean) value 2 bytes – maximum value 2 bytes – an optional current value The maximum number of objects depends on the size of the EPL and the optional current value present bit value. If multiple A0h-AFh pages are present then the data is expected to be contiguous across pages. The first PM object data is from the lowest bit set to 1b in the lane bitmask. i.e. the first bit set to 1b starting from Bytes 144-155 of this 0215h command.	

9.7.6 CMD 0216h/0217h: Data Path Related LPL/EPL

Table 9-33 CDB Command 0216/0217h: Data Path Related LPL/EPL

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Data Path PM using LPL	0216h
			Data Path PM using EPL	0217h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	14h
9Fh	133	CdbChkCode	Bytes 128 to 155 calculated with Bytes 133-135=0	
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136	Clear latch Mode	Bit 0: 0b: PM Object consists of 6 bytes (minimum, average and maximum) 1b: PM object consists of 8 bytes and includes a “current” value. Bit 1-5: Reserved Bit 7: 0b: return the PM data 1b: return the selected PM data and then reset the latching of the selected PM data.	
9Fh	137-139	Reserved	Reserved for modules with more than 32 lanes.	
9Fh	140	Bitmask DID 32-25	Bitmask indicating which data path ID (DID) is present. These encoding allow for Bytes 140-143 to be interpreted as a 32 bit Big Endian word, (bit 0 represents lane 1 and bit 31 represent lane 32).	
9Fh	141	Bitmask DID 24-17		
9Fh	142	Bitmask DID 16-9		
9Fh	143	Bitmask DID 8-1		
9Fh	144	Selected PM data	Bit 0: Errored Frame Rate (uncorrectable frames) Bit 1: Media Side PreFEC BER Bits 2-7 : Reserved	
9Fh	145-147	Selected PM data	Reserved.	
9Fh	148-151	Selected PM data	Reserved for Coherent.	
9Fh	152-155	Selected PM data	Reserved for Vendor.	
CDB flags and status fields				
00h	8	CDB complete flag	CDB complete flag is set when command has completed.	
00h	37 or 38	CDB Status	**In Progress** 10 000001b=Busy processing command, CMD captured 10 000010b=Busy processing command, CMD checking 10 000011b=Busy processing command, CMD execution **On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b=CdbChkCode error 01 000110b=Password error – insufficient privilege	

Page	Byte	Name	Description	Value
Returned Data Path Lane PM Using LPL (0216h)				
9Fh	136-255	LPL PM data (up to 120 bytes)	Module PM object of one PM parameter consists of 6 to 8 bytes. 2 bytes – minimum value 2 bytes – average (mean) value 2 bytes – maximum value 2 bytes – an optional current value A maximum of 15 to 20 objects can be returned using LPL depending if the optional current value is present. The first PM object data is from the lowest set bit in the DID bitmask, of ('or')the first bit set starting from Bytes 144-155 of this 0216h command.	
Returned Data Path Lane PM Using EPL (0217h)				
A0h to AFh	128-255	EPL PM data (number of bytes depends on available pages)	Module PM object of one PM parameter consists of 6 to 8 bytes. 2 bytes – minimum value 2 bytes – average (mean) value 2 bytes – maximum value 2 bytes – an optional current value The maximum number of objects depends on the size of the EPL and the optional current value present bit value. If multiple A0h-AFh pages are present then the data is expected to be contiguous across pages. The first PM object data is from the lowest set bit in the DID bitmask, of ('or')the first bit set starting from Bytes 144-155 of this 0217h command.	

9.8 CDB Data Monitoring and Recording

Table 9-34 CDB Data Monitoring and Recording Commands Overview

Cmd Code	Name	Description	Type	Section
0280h	Data Monitoring Controls		Req	10.8.1
0281h	Advertisement		Opt	10.8.2
0282h-02FFh	Reserved			
0290h	Temperature Histogram		Opt	10.8.3
0291h-02FFh	Reserved			

9.8.1 CMD 0280h: Data Monitoring and Recording Controls

Table 9-35 CDB Command 0280h: Data Monitoring and Recording Controls

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Data Monitoring Controls	0280h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	04h
9Fh	133	CdbChkCode	Bytes 128 to 139 calculated with Bytes 133-135=0	
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136	Mode		
9Fh	137	Reserved		00h
9Fh	138	Clear All Latches all Lanes	Bit 0 0b: No operation. This command is used to change other control attributes. 1b: Clear all minimum, average, maximum latches for all managed parameters for all lanes at the same time as best as possible. Bit 1-7 Reserved. Set to 0.	
9Fh	139	Reserved		00h
9Fh	140-255	Reserved	Not sent	
CDB flags and status fields				
00h	8	CDB complete flag	This command does not assert the CDB complete flag and will NACK until command is completed.	
00h	37 or 38	CDB Status	**On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b=CdbChkCode error 01 000110b=Password error – insufficient privilege	
Module return LPL				
9Fh	136-255	Reserved.		

9.8.2 CMD 0281h: Data Monitoring and Recording Advertisement.

Table 9-36 CDB Command 0281h: Data Monitoring and Recording Advertisement

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code	Reserved for advertisement of the PM features defined in CMDs 0290-029Fh	0281h
9Fh	130-131	EPL Len	EPL is not used for this command.	0000h
9Fh	132	LPL Len	Length of LPL for this command	00h
9Fh	133	CdbChkCode	Bytes 128 to 135 calculated with Bytes 133-135=0	7Ch
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136-255	Reserved	Not sent	
CDB flags and status fields				
00h	8	CDB complete flag	This command does not assert the CDB complete flag and will NACK until command is completed.	
00h	37 or 38	CDB Status	**On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b=CdbChkCode error 01 000110b=Password error – insufficient privilege	
Module return LPL				
9Fh	136-255	Reserved.	Reserved for PAM4 histogram	

9.8.3 CMD 0290h: Temperature Histogram

This is an optional feature of a module to track the number of seconds in non volatile memory, in which the module has operated within the defined temperature bins, since the last time the host or user has cleared the temperature histogram. The sampling interval and interval at which the module writes to non volatile memory is module dependent. In order for the host not to lose any histogram data, the host may send a command to "write" the current histogram to NVR before decommissioning or unplugging a module from its slot. The timing accuracy of the internal clock is not defined here.

Table 9-37 CDB Command 0290h: Temperature Histogram

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code		0290h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	01h
9Fh	133	CdbChkCode	Bytes 128 to 136 calculated with Bytes 133-135=0	
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136	Selected PM data	Bit 0: Reserved Bit 1: Write current histogram to NVR Bit 2: 10C bins Bit 3-6: Reserved Bit 7: Clear Temperature Histogram (should be non-volatile)	
9Fh	137-255	Reserved		
CDB flags and status fields				
00h	8	CDB complete flag	CDB complete flag is set when command has completed.	
00h	37 or 38	CDB Status	**In Progress** 10 000001b=Busy processing command, CMD captured 10 000010b=Busy processing command, CMD checking 10 000011b=Busy processing command, CMD execution **On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b= CdbChkCode error 01 000110b=Password error – insufficient privilege	
Module return LPL				
9Fh	136	Selected PM data	Echo of host-written values	
9Fh	137	Number of Hours before Next Write	0: Module does not indicate when it will write to the NVR next. 1-254: Temperature Histogram will be written to NVR within this specified number of hours. NOTE: Depends on device technology use, NVR writes may need to be triggered by host. 255: NVR write needs to be triggered by host. If the module were to write NVR autonomously, some operations may share EEPROM or flash device and may cause smaller microcontrollers to stop responding to TWI while the autonomous write is in progress.	

Page	Byte	Name	Description	Value
9Fh	138-139	Reserved		
9Fh	140-143	Total Seconds	Total number of seconds temperature histogram has been accumulating.	
9Fh	144-147	Seconds Temp < -5.0	Total number of seconds module operated within this temperature region.	
9Fh	148-151	Seconds -5.0 <= Temp < 5.0	Total number of seconds module operated within this temperature region.	
9Fh	152-155	Seconds 5.0 <= Temp < 15.0	Total number of seconds module operated within this temperature region.	
9Fh	156-159	Seconds 15.0 <= Temp < 25.0	Total number of seconds module operated within this temperature region.	
9Fh	160-163	Seconds 25.0 <= Temp < 35.0	Total number of seconds module operated within this temperature region.	
9Fh	164-167	Seconds 35.0 <= Temp < 45.0	Total number of seconds module operated within this temperature region.	
9Fh	168-171	Seconds 45.0 <= Temp < 55.0	Total number of seconds module operated within this temperature region.	
9Fh	172-175	Seconds 55.0 <= Temp < 65.0	Total number of seconds module operated within this temperature region.	
9Fh	176-179	Seconds 65.0 <= Temp < 75.0	Total number of seconds module operated within this temperature region.	
9Fh	180-183	Seconds 75.0 <= Temp < 85.0	Total number of seconds module operated within this temperature region.	
9Fh	184-187	Seconds Temp >= 85.0	Total number of seconds module operated within this temperature region.	

9.9 CDB PRBS BERT

To be defined. Currently all these features are available using pages 13h/14h.

Table 9-38 CDB BERT Commands Overview

CMD Code	Name	Description	Type	Section
0300h	PRBS Capabilities	Advertise Capabilities		
030xh	PRBS Generator	PRBS Generator Config, Enable and Disable		
030xh	PRBS Generator Error Injector			
030xh	PRBS Detector	PRBS Detector (Checker) Config, Enable and Disable		
030xh	PRBS Error Counts			
030xh	PRBS BER			
030xh-037Fh	Reserved			

9.10 CDB Diagnostics and Debug

Table 9-39 CDB Diagnostics and Debug Commands Overview

CMD Code	Name	Description	Type	Section
0380h	Loopbacks	See below		
0390h	PAM4 Histogram	TBD		
03A0h	Eye Monitors			

9.10.1 CMD 0380h: Loopbacks

Basic loopback modes are available using features implemented in 13h/14h. This command is reserved for additional loopback capabilities.

Table 9-40 CDB Command 0380h: Loopbacks

Page	Byte	Name	Description	Value
CDB command fields				
9Fh	128-129	CMD Code		0380h
9Fh	130-131	EPL Len	EPL is not used for this command	0000h
9Fh	132	LPL Len	Length of LPL for this command.	00h
9Fh	133	CdbChkCode	Bytes 128 to 135 calculated with Bytes 133-135=0	7Ch
9Fh	134	RLPLLen	See Table 8-106	
9Fh	135	RLPLChkCode	See Table 8-106	
Host-written LPL				
9Fh	136-255	Reserved		
CDB flags and status fields				
00h	8	CDB complete flag	CDB complete flag is set when command has completed.	
00h	37 or 38	CDB Status	**In Progress** 10 000001b=Busy processing command, CMD captured 10 000010b=Busy processing command, CMD checking 10 000011b=Busy processing command, CMD execution **On Success** 00 000001b=Success, no specific message **On Failure** 01 000000b=Failed, no specific failure code 01 000010b=Parameter range error or not supported 01 000101b=CdbChkCode error 01 000110b=Password error – insufficient privilege	
Module return LPL				
9Fh	136-255	Reserved		

Appendix A Form Factor Specific Signal Names

Table A-1 associates form factor-specific terminology and signal names for four form factors with the generic terms used in this specification.

Table A-1 Form Factor Signal Name Associations

CMIS generic name	QSFP-DD	QSFP	OSFP	COBO
ResetL	ResetL	ResetL	RSTn	ResetL
Interrupt	IntL	IntL	INT	IntL
LPMode	LPMode	LPMode	LPWn	LPMode

Appendix B Examples of Application Advertisements

Table B-1 400GBASE-DR4 Application Advertising Example illustrates an example module advertisements for a 400GBASE-DR4 transceiver that also supports aggregation of four 100G interfaces. With this example, the host could select either ApSel 1 or ApSel 2 in one of the Staged Control Sets. ApSel 1 (400GAUI-8 to 400GBASE-DR4) is the default application populated in the Active Set at power-on.

Table B-1 400GBASE-DR4 Application Advertising Example

Byte	Bits	ApSel Code	Name	Value	Description
85	7-0	N/A	Module Type encoding	02h	Optical Interfaces: SMF
86	7-0	0001b	Host Electrical Interface ID	11h	400GAUI-8 C2M
87	7-0		Module Media Interface ID	13h	400GBASE-DR4
88	7-4		Host Lane Count	8	8 host electrical lanes
	3-0		Media Lane Count	4	4 module media lanes
89	7-0		Host Lane Assignment Options	01h	Permissible first host lane number for Application: lane 1
176 Page 01h	7-0		Media Lane Assignment Options	01h	Permissible first media lane number for Application: lane 1
90	7-0	0010b	Host Electrical Interface ID	0Dh	100GAUI-2 C2M
91	7-0		Module Media Interface ID	14h	100GBASE-DR
92	7-4		Host Lane Count	2	2 host electrical lanes
	3-0		Media Lane Count	1	1 module media lane
93	7-0		Host Lane Assignment Options	55h	Permissible first host lane number for Application: lanes 1, 3, 5, and 7
177 Page 01h	7-0		Media Lane Assignment Options	0Fh	Permissible first media lane number for Application: lanes 1, 2, 3, 4
94	7-0	0011b	Host Electrical Interface ID	FFh	End of list of supported Applications
95	7-0		Module Media Interface ID	00h	
96	7-4		Host Lane Count	0	
	3-0		Media Lane Count	0	
97	7-0		Host Lane Assignment Options	00h	
178 Page 01h	7-0		Media Lane Assignment Options	00h	

Table B-2 400G-SR8 only Transceiver Application Advertising Example illustrates an example module advertisement for a 400GBASE-SR8 transceiver that does not support other Applications. With this example, the host can select only ApSel 1 in one of the Staged Control Sets

Table B-2 400G-SR8 only Transceiver Application Advertising Example

Byte	Bits	ApSel Code	Name	Value	Description
85	7-0	N/A	Module Type encoding	01h	Optical Interfaces: MMF
86	7-0	0001b	Host Electrical Interface ID	11h	400GAUI-8 C2M
87	7-0		Module Media Interface ID	10h	400G-SR8
88	7-4		Host Lane Count	8	8 host electrical lanes
	3-0		Media Lane Count	8	8 module media lanes
89	7-0		Host Lane Assignment Options	01h	Permissible first host lane number for Application: lane 1
176 Page 01h	7-0		Media Lane Assignment Options	01h	Permissible first media lane number for Application: lane 1
90	7-0	0010b	Host Electrical Interface ID	FFh	End of list of supported Applications
91	7-0		Module Media Interface ID	00h	
92	7-4		Host Lane Count	0	
	3-0		Media Lane Count	0	
93	7-0		Host Lane Assignment Options	00h	
177 Page 01h	7-0		Media Lane Assignment Options	00h	

Table B-3 400G-SR8 Transceiver supporting 200G-SR4, 100G-SR2 and 50G-SR Advertising Exampleillustrates an example module advertisement for an 8x50G transceiver that supports breakout to a variety of lane widths. With this example, the host could select either ApSel 1, 2, 3, or 4 in one of the Staged Control Sets, where ApSel 1 (400GAUI-8 to 400G-SR8) is the default application populated in the Active Set at power-on.

Table B-3 400G-SR8 Transceiver supporting 200G-SR4, 100G-SR2 and 50G-SR Advertising Example

Byte	Bits	ApSel Code	Name	Value	Description
85	7-0	N/A	Module Type encoding	01h	Optical Interfaces: MMF
86	7-0	0001b	Host Electrical Interface ID	11h	400GAUI-8 C2M
87	7-0		Module Media Interface ID	10h	400G-SR8
88	7-4		Host Lane Count	8	8 host electrical lanes
	3-0		Media Lane Count	8	8 module media lanes
89	7-0		Host Lane Assignment Options	01h	Permissible first host lane number for Application: lane 1
176 Page 01h	7-0		Media Lane Assignment Options	01h	Permissible first media lane number for Application: lane 1
90	7-0	0010b	Host Electrical Interface ID	0Fh	200GAUI-4 C2M
91	7-0		Module Media Interface ID	0Eh	200GBASE-SR4
92	7-4		Host Lane Count	4	4 host electrical lanes
	3-0		Media Lane Count	4	4 module media lanes
93	7-0		Host Lane Assignment Options	11h	Permissible first host lane number for Application: lanes 1 and 5
177 Page 01h	7-0		Media Lane Assignment Options	11h	Permissible first media lane number for Application: lanes 1, 5
94	7-0	0011b	Host Electrical Interface ID	0Dh	100GAUI-2 C2M
95	7-0		Module Media Interface ID	0Ch	100GBASE-SR2
96	7-4		Host Lane Count	2	2 host electrical lanes
	3-0		Media Lane Count	2	2 module media lanes
97	7-0		Host Lane Assignment Options	55h	Permissible first host lane number for Application: lanes 1, 3, 5, and 7
178 Page 01h	7-0		Media Lane Assignment Options	55h	Permissible first media lane number for Application: lanes 1, 3, 5, 7
98	7-0	0100b	Host Electrical Interface ID	0Ah	50GAUI-1 C2M
99	7-0		Module Media Interface ID	07h	50GBASE-SR
100	7-4		Host Lane Count	1	1 host electrical lane
	3-0		Media Lane Count	1	1 module media lane
101	7-0		Host Lane Assignment Options	FFh	Permissible first host lane number for Application: lanes 1, 2, 3, 4, 5, 6, 7, 8
179 Page 01h	7-0		Media Lane Assignment Options	FFh	Permissible first media lane number for Application: lanes 1, 2, 3, 4, 5, 6, 7, 8
102	7-0	0101b	Host Electrical Interface ID	FFh	End of list of supported Applications
103	7-0		Module Media Interface ID	00h	
104	7-4		Host Lane Count	0	
	3-0		Media Lane Count	0	
105	7-0		Host Lane Assignment Options	00h	
180 Page 01h	7-0		Media Lane Assignment Options	00h	

Table B-4 8x50G AOC Application Advertising Exampleillustrates an example module advertisement for an 8x50G AOC that supports one 8x50G host electrical interface or two 4x50G host electrical interfaces. With this example, the host could select either ApSel 1 or ApSel 2 in one of the Staged Control Sets. ApSel 1 (400GAUI-8) is the default application populated in the Active Set at power-on.

Table B-4 8x50G AOC Application Advertising Example

Byte	Bits	ApSel Code	Name	Value	Description
85	7-0	N/A	Module Type encoding	04h	Active cables
86	7-0	0001b	Host Electrical Interface ID	11h	400GAUI-8 C2M
87	7-0		Module Media Interface ID	03h	AOC with BER < 2.4e-4
88	7-4		Host Lane Count	8	8 host electrical lanes
	3-0		Media Lane Count	8	8 module media lanes
89	7-0		Host Lane Assignment Options	01h	Permissible first host lane number for Application: lane 1
176 Page 01h	7-0		Media Lane Assignment Options	01h	Permissible first media lane number for Application: lane 1
90	7-0	0010b	Host Electrical Interface ID	0Fh	200GAUI-4 C2M
91	7-0		Module Media Interface ID	03h	AOC with BER < 2.4e-4
92	7-4		Host Lane Count	4	4 host electrical lanes
	3-0		Media Lane Count	4	4 module media lanes
93	7-0		Host Lane Assignment Options	11h	Permissible first host lane number for Application: lanes 1 and 5
177 Page 01h	7-0		Media Lane Assignment Options	11h	Permissible first media lane number for Application: lanes 1, 5
94	7-0	0011b	Host Electrical Interface ID	FFh	End of list of supported Applications
95	7-0		Module Media Interface ID	00h	
96	7-4		Host Lane Count	0	
	3-0		Media Lane Count	0	
97	7-0		Host Lane Assignment Options	00h	
178 Page 01h	7-0		Media Lane Assignment Options	00h	

Appendix C Example Initialization Flows

This appendix includes some example flows that illustrate interactions between the host and module during module and data path initialization. Refer to section 6.3.1 for Module State Machine details and section 6.3.2 for Data Path State Machine, Application, and Control Set details.

C.1 Host Flow Examples

This section contains example flows that could be used by host implementers to power up and initialize the module and example flows that could be used by host implementers to deinitialize and power down the module.

The following example host flows are in this section.

Name	Description	Section
Quick hardware initialization	Flow showing power up and initialization with no host software interaction	C.1.1
Quick software initialization	Flow showing power up and initialization with minimal host software interaction	C.1.2
Software configuration and initialization	Flow showing power up and initialization with module configuration by host software interaction	C.1.3
Hardware deinitialization	Flow showing power-down sequence using hardware control	C.1.4
Software deinitialization	Flow showing power-down sequence using software control	C.1.5

C.1.1 Quick Hardware Initialization

The following table provides an example of a simple module power-up sequence where the module powers up under hardware control (LPMode=0) without host software intervention. This example flow has the following key attributes:

a. Module is powered-up from an un-powered state
b. Module is powered-up under hardware control (LPMode=0)
c. Host uses the default settings for the selected Application. The host does not use custom signal integrity settings (i.e. Explicit Control indicator)
d. Host does not perform speed negotiation

#	Host Action	Module Action	Module State (M) Data Path State (D)
0	Host applies Vcc, LPMode=0, ResetL=1. Host must also ensure that host transmitters are configured to produce a stable signal that is consistent with the default Application in the module, prior to step 7 below.		
1	Hot Plug		
2	Host detects module presence, waits for IntL assertion	Module powers up and initializes management interface, setting ForceLowPwr=0, LowPwr=1 and DataPathDeinit=00h and writing the power on default data path configurations into the Active Set and Staged Set 0	M=MgmtInit D=DataPathDeactivated

#	Host Action		Module Action	Module State (M) Data Path State (D)
3			Module sees LowPwrS transition signal is FALSE on entry into ModuleLowPwr and transitions to ModulePwrUp	M=ModuleLowPwr D=DataPathDeactivated
4			Module powers up to High Power Mode	M=ModulePwrUp D=DataPathDeactivated
5			Module sets the Module State Changed flag to 1 on entry into ModuleReady	M=ModuleReady D=DataPathDeactivated
6	Host detects assertion of IntL and reads all interrupt flag registers, which deasserts IntL		Module sees DataPathDeinitS transition signal is FALSE and transitions all data path states to DataPathInit	
7	Host waits for second IntL assertion to indicate completion of data path initialization		Module initializes all data paths according to the configuration in the Active Set.	M=ModuleReady D=DataPathInit
8			Module sees DataPathDeactivateS transition signal is FALSE and transitions all data path states to DataPathTxTurnOn	M=ModuleReady D=DataPathInitialized
9			Modules enables all Tx outputs	M=ModuleReady D=DataPathTxTurnOn
10			Module sets the Data Path State Changed interrupt flags to 1 on entry into DataPathActivated	M=ModuleReady D=DataPathActivated
11	Host detects assertion of IntL and reads all interrupt flag registers, which deasserts IntL	<-	Module waits for host action	

C.1.2 Quick Software Initialization

The following table provides an example of a simple module power-up sequence where the module powers up under software control (LPMode=1) but uses the default data path configuration. This example flow has the following key attributes:

a. Module is powered-up from an un-powered state
b. Module is powered-up under software control (LPMode=1)
c. Host uses the default settings for the selected Application. The host does not use custom signal integrity settings (i.e. Explicit Control indicator)
d. Host does not perform speed negotiation

#	Host Action		Module Action	Module State (M) Data Path State (D)
0	Host applies Vcc, LPMode=1, ResetL=1			
1	Hot Plug			

#	Host Action		Module Action	Module State (M) Data Path State (D)
2	Host detects module presence, waits for IntL assertion		Module powers up and initializes management interface, setting ForceLowPwr=0, LowPwr=1 and DataPathDeinit=00h and writing the power on default data path configurations into the Active Set and Staged Set 0	M=MgmtInit D=DataPathDeactivated
3		<-	Module sets the Module State Changed flag to 1 on entry into ModuleLowPwr	M=ModuleLowPwr D=DataPathDeactivated
4	Host detects assertion of IntL and reads the interrupt flag registers, which deasserts IntL		Module waits for host action	
5	Host reads module power requirements and data path configuration information			
6	Host configures and enables host transmitters such that they are producing a stable signal that is consistent with the default Application in the module			
7	Host sets LowPwr bit to 0 to initiate a module transition to High Power Mode	->		
8	Host waits for IntL assertion to indicate completion of transition to High Power Mode		Module sees LowPwrS transition signal become FALSE and transitions to ModulePwrUp	
9			Module powers up to High Power Mode	M=ModulePwrUp D=DataPathDeactivated
10			Module sets the Module State Changed flag to 1 on entry into ModuleReady	M=ModuleReady D=DataPathDeactivated
11	Host detects assertion of IntL and reads all interrupt flag registers, which deasserts IntL		Module sees DataPathDeinitS transition signal is FALSE and transitions all data path states to DataPathInit	
12	Host waits for second IntL assertion to indicate completion of data path initialization		Module initializes all data paths according to the configuration in the Active Set.	M=ModuleReady D=DataPathInit
13			Module sees DataPathDeactivateS transition signal is FALSE and transitions all data path states to DataPathTxTurnOn	M=ModuleReady D=DataPathInitialized
14			Modules enables all Tx outputs	M=ModuleReady D=DataPathTxTurnOn
15		<-	Module sets the Data Path State Changed interrupt flags to 1 on entry into DataPathActivated	M=ModuleReady D=DataPathActivated
16	Host detects assertion of IntL and reads all interrupt flag registers, which deasserts IntL		Module waits for host action	

C.1.3 Software Configuration and Initialization

The following table provides an example of a simple module power-up sequence where the module powers up under software control (LPMode=1). In this example, host software powers up the module and the data paths in two separate steps. This example flow has the following key attributes:

a. Module is powered-up from an un-powered state
b. Module is powered-up under host software control (LPMode=1)
c. Host selects one of the Applications advertised by the module
d. Host uses the default settings for the selected Application. The host does not use custom signal integrity settings (i.e. Explicit Control indicator)
e. Host uses only staged Control Set 0 to configure the module (optional Staged Control Set 1 is not used).
f. Host does not perform speed negotiation

#	Host Action		Module Action	Module State (M) Data Path State (D)
0	Host applies Vcc, LPMode=1, ResetL=1			
1	Hot Plug			
2	Host detects module presence, waits for IntL assertion		Module powers up and initializes management interface, setting ForceLowPwr=0, LowPwr=1 and DataPathDeinit=00h and writing the power on default data path configurations into the Active Set and Staged Set 0	M=MgmtInit D=DataPathDeactivated
3		<-	Module sets the Module State Changed flag to 1 on entry into ModuleLowPwr	M=ModuleLowPwr D=DataPathDeactivated
4	Host detects assertion of IntL and reads all interrupt flag registers, which deasserts IntL		Module waits for host action	
5	Host reads module power requirements			
6	Host writes FFh to the DataPathDeinit register to prevent automatic data path initialization when the module state reaches ModuleReady			
7	Host sets LowPwr bit to 0 to initiate a module transition to High Power Mode	->		
8	Host waits for IntL assertion to indicate completion of transition to High Power Mode		Module sees LowPwrS transition signal become FALSE and transitions to ModulePwrUp	
9			Module powers up to High Power Mode	M=ModulePwrUp D=DataPathDeactivated
10		<-	Module sets the Module State Changed flag to 1 on entry into ModuleReady	M=ModuleReady D=DataPathDeactivated
11	Host detects assertion of IntL and reads all interrupt flag registers, which deasserts IntL		Module waits for host action	
12	Host reads Application advertising registers			

#	Host Action		Module Action	Module State (M) Data Path State (D)
13	Host writes desired ApSel code into applicable Application registers in Staged Set 0			
14	Host configures and enables host transmitters such that they are producing a stable signal that is consistent with the selected Application			
15	Host writes FFh to Apply_DataPathInit to request that the new configuration be committed to the Active Set	->		
16			Module validates the configuration requested in Staged Control Set 0. If the configuration was found to be valid, the module copies the contents to the Active Control Set. If the configuration was found to be invalid the module sets the appropriate bytes in the Configuration Error Code fields.	
		<-		
17	Host reads the Configuration Error Code fields to confirm that the requested configuration was verified and accepted by the module for all associated lanes of the selected Application.		Module waits for host action	
18	Host requests initialization of the newly configured data path by writing 00h to DataPathDeinit	->		
19	Host waits for IntL assertion to indicate completion of data path initialization		Module sees DataPathDeinitS transition signal is FALSE and transitions all data path states to DataPathInit	
20			Module initializes all data paths according to the configuration in the Active Set.	M=ModuleReady D=DataPathInit
21			Module sees DataPathDeactivateS transition signal is FALSE and transitions all data path states to DataPathTxTurnOn	M=ModuleReady D=DataPathInitialized
22			Modules enables all Tx outputs	M=ModuleReady D=DataPathTxTurnOn
23			Module sets the Data Path State Changed interrupt flags to 1 on entry into DataPathActivated	M=ModuleReady D=DataPathActivated
		<-		
24	Host detects assertion of IntL and reads all interrupt flag registers, which deasserts IntL		Module waits for host action	

C.1.4 Hardware Deinitialization

The following table provides an example of a simple module power-down sequence where the module powers down under hardware control (LPMode transitions from 0 to 1) without software interaction. This example flow has the following key attributes:

a. Module was previously powered up under hardware control (LPMode=0)
b. At least one data path is in the DataPathActivated state

#	Host Action		Module Action	Module State (M) Data Path State (D)
0	Module is powered up with at least one data path activated. LPMode = 0, ResetL = 1		Initial conditions: Module fully configured and powered	M=ModuleReady D=DataPathActivated
1	The host releases the LPMode signal (LPMode = 1)	->	Module sees DataPathDeactivateS transition signal is TRUE and transitions all data path states to DataPathTxTurnOff	
2			Since all Tx Disable and Tx Force Squelch bits are 0, all data path states transition to DataPathInitialized without any other action	M=ModuleReady D=DataPathTxTurnOff
3			Module sees DataPathReDeinitS is TRUE and transitions all data path states to DataPathDeinit	M=ModuleReady D=DataPathInitialized
4			Module deinitializes data path resources	M=ModuleReady D=DataPathDeinit
5			Module sets the Data Path State Changed interrupt flags to 1 on entry into DataPathDeactivated	M=ModuleReady D=DataPathDeactivated
6	Host detects assertion of IntL and reads all interrupt flag registers, which deasserts IntL		Module sees LowPwrExS is TRUE and transitions the module state to ModulePwrDn	
7	Host waits for second IntL assertion to indicate completion of module power down		Module reduces the module power to low power mode levels	M=ModulePwrDn D=DataPathDeactivated
8		<-	Module sets the Module State Changed interrupt flag to 1 on entry into ModuleLowPwr	M=ModuleLowPwr D=DataPathDeactivated
9	Host detects assertion of IntL and reads all interrupt flags to clear the interrupt		Module waits for host action	

C.1.5 Software Deinitialization

The following table provides an example of a simple module power-down sequence where the module powers down under software control (LPMode=1). This example flow has the following key attributes:

a. Module was previously powered up under software control (LPMode=1)
b. At least one data path is in the DataPathActivated state

#	Host Action		Module Action	Module State (M) Data Path State (D)
0	Module is powered up with at least one data path activated. LPMode = 1, ResetL = 1		Initial condition: Module fully configured and powered	M=ModuleReady D=DataPathActivated
1	The host sets the DataPathDeinit bit for all host lanes in the applicable data path to 1	->	Module sees DataPathDeactivateS transition signal is TRUE and transitions all data path states to DataPathTxTurnOff	
2			Since all Tx Disable and Tx Force Squelch bits are 0, all data path states transition to DataPathInitialized without any other action	M=ModuleReady D=DataPathTxTurnOff
3			Module sees DataPathReDeinitS is TRUE and transitions all data path states to DataPathDeinit	M=ModuleReady D=DataPathInitialized
4			Module deinitializes data path resources	M=ModuleReady D=DataPathDeinit
5		<-	Module sets the Data Path State Changed interrupt flags to 1 on entry into DataPathDeactivated	M=ModuleReady D=DataPathDeactivated
6	Host detects assertion of IntL and reads all interrupt flag registers, which deasserts IntL		Module waits for host action	
7	Host sets the LowPwr bit to 1	->	Module sees LowPwrExS is TRUE and transitions the module state to ModulePwrDn	
8	Host waits for IntL assertion to indicate completion of module power down		Module reduces the module power to low power mode levels	M=ModulePwrDn D=DataPathDeactivated
9		<-	Module sets the Module State Changed interrupt flag to 1 on entry into ModuleLowPwr	M=ModuleLowPwr D=DataPathDeactivated
10	Host detects assertion of IntL and reads all interrupt flags to clear the interrupt		Module waits for host action	

Appendix D Examples of Diagnostic Features Usage

This Appendix contains usage recommendations for the diagnostic features on pages 13h and 14h. For use of these diagnostic features the module should be in the Module Ready state with a selected application. The data path state is not defined for these diagnostic features.

D.1 Enabling and Disabling Host (or Media) Pattern Generator

The following procedure contains the recommended set of host TWI transactions to set the module into Host side (or Media side) pattern generation mode. Host side registers are provided, with media side registers in parenthesis.

1. Write the bank and page select registers to select page 13h on the appropriate bank.
2. Set byte 177 Page 13h to desired mode of operation.
3. Write bytes 145-151 (153-159) on page 13h with the desired pattern generator configuration and lane pattern.
4. Write bytes 176-179 on page 13h with the desired control options.
5. Write byte 144, bits 7-0 (152) on page 13h to enable the pattern generator on the selected lanes.

After the above sequence of commands, the host side electrical (media side electrical or optical) output will be generating the selected pattern for the enabled lanes. NOTE: The pattern generation feature may vary by module. On some modules, when in pattern generation mode, per lane control is not provided and all lanes may be generating the pattern. On other modules, such as modules design to support break-out, the selected lanes may be in pattern generation mode while other lanes are either disabled or in normal mission mode.

6. Write byte 144, bits 7-0 (152) on page 13h to disable the pattern generator on selected host side (media side) lanes.

When pattern generation is disabled on selected lanes, those lanes are expected to revert to mission mode if possible. In some modules, mission mode can only be achieved if none of the module interfaces, host side or media side are in pattern generation mode. A module reset may be used to guarantee that the module reverts back to mission mode. Otherwise, the host has to ensure that all pattern generation modes on all lanes for both the host and media sides are disabled for these types of modules.

D.2 Enabling Host (Media) Interface Pattern Checker

The following procedure contains the recommended set of host TWI transactions to set the module into Host side (or Media side) pattern generation mode. Host side registers are provided, with media side registers in parenthesis.

1. Write the bank and page select registers to select page 13h on the appropriate bank.
2. Set byte 177 page 13h for desired mode of operation.
3. Write bytes 161-167 (169-175) on page 13h with the desired pattern checker configuration and lane pattern.
4. Write bytes 176-179 on page 13h with the desired control options.
5. Write byte 160, bits 7-0 (168) on page 13h to enable the pattern checker on the selected lanes.

When the host enables the PRBS checker, the module is expected to reset the error counters and enable the error counters to begin counting. The behavior of the error counters is defined by byte 177 on page 13h. The following section details some of the error counter configurations and their expected behavior.

To disable the pattern checker (at any time) including in the middle of a gated error count operation, the host may set byte 160, bits 7-0 (168) to 0. If the pattern checker is disabled in the middle of a gated operation, all of the error counters are undefined. Disabling in the middle of a gated count is considered an abort operation by the module.

D.2.1 Reading Pattern Checker Error Counters

There are many scenarios in which the pattern checker can be used, based on the configuration in byte 177 on page 13h. The following sections describe the recommended host write sequences for some commonly used scenarios. These recommended sequences are provided so that host and module vendors can align on usage methods to ensure compatibility across a variety of hosts and modules. Media side registers are provided in the illustrations, but these same sequences can also be applied to host side registers. The example Application for these sequences has 8 host side lanes and 4 media side lanes.

D.2.2 Not Gated (Continuous) Error Counters, Individual Lanes,

Host Selected Mode of Operation :

a. Page 13h, byte 177, bits 3-1 = 0 (not gated)
b. Page 13h, byte 177, bit 5 = 0 (do not hold checkers in reset)
c. Page 13h, byte 177, bit 7 = 0 (reset error counts per lane)
d. Page 13h, byte 129, bit 4 = 0
    - Page 13h, byte 177, bit 0 = X. (disable)

13h13h

Host write sequence:

1. Write byte 160, bits 7-0 (168) on page 13h to enable the pattern checker on selected media side lanes.
    a. The module will apply the configuration and control options to the enabled lanes.
    b. Since the configuration is not gated and polling is disabled, the Latest Error counters are available “on demand” when the host reads the current pattern checker data.
2. Write 14h to the page select register. Since error information is on demand, module may take additional time to respond with the selected diagnostics data.
3. Write the Diagnostics Selector in byte 128 on page 14h to 02h (04h) to select lanes 1-4 for the host side (media side) or write a 03h (05h) to select lanes 5-8 (e.g. for DR4, FR4, LR4)
4. Module will perform a read of the pattern checker error counters when byte 128 is written. (Module will not clear the error counters.)
5. Read byte 138 (139) on page 14h to ensure the pattern checker has not lost lock.
6. Read bytes R192-255 to obtain error counters and total bits.

D.2.3 Not Gated (Continuous) Error Counters, Individual Lanes, Reset Error Counter

Configuration assumptions:

a. Page 13h, byte 177, bits 3-1 = 0 (not gated)
e. Page 13h, byte 177, bit 5 = 0 (do not hold checkers in reset)
f. Page 13h, byte 177, bit 7 = 0 (reset error counts per lane)
g. Page 13h, byte 129, bit 4 = 1 (polling enabled)
    - Page 13h, byte 177, bit 0 = 0. (poll every 1 sec.)

Host write sequence:

1. Write byte 160, bits 7-0 (168) on page 13h to enable the pattern checker on selected media side lanes.
    a. The module will apply the configuration and control options to the enabled lanes.
    b. Since the configuration is not gated and polling is enabled, the module may provide the error information from the last polling period.
    c. Error counters may also available “on demand” when the host reads the current pattern checker data but this behavior is purposely left to be vendor dependent.
2. Write 14h to the page select register. To provide better response to host, the module may return the last polled error information.
3. Write the Diagnostics Selector in byte 128 on page 14h to 02h (or 04h) to select lanes 1-4 for the host side (media side) or write a 03h (05h) to select host (media) lanes 5-8 (e.g. for DR8, FR8, LR8)
4. Read byte 138 (139) on page 14h to ensure the pattern checker has not lost lock.
5. If the host wants to reset the error information, the host shall set 13h.Byte177.Bit5 to 1. When set:
    a. Module (may also read from the data path chips and then) freezes the current error information.
    b. Module copies current internal pattern checker counters into the latched counters.

6. Host may write the Diagnostics Selector in byte 128 on page 14h to 11h-15h to select and read the latched error information, by reading bytes 192-255 in Page 14h for the latched BER, error counters and total bits.
7. If the host wants to restart the error counter, the host shall set 13h.Byte177.Bit5 to 0. This will reset the current error information in selector 01h-05h without affecting the latched error information in 11h-15h.

D.2.4 Not Gated (Continuous) Error Counters, All Lanes, all banks

Configuration assumptions:

a. Page 13h, byte 177, bits 3-1 = 0 (not gated)
b. Page 13h, byte 177, bit 5 = 0 (do not hold checkers in reset)13h
c. Page 13h, byte 177, bit 7 = 1 (reset error counts on all banks all enabled lane)13h
d. Page 13h, byte 129, bit 4 = 0 (polling enabled)
    - Page 13h, byte 177, bit 0 = 1. (poll every 5 sec.)13h

Host write sequence:

1. Write byte 160, bits 7-0 (168) on page 13h to enable the pattern checker on selected media side lanes.
    a. The module will apply the configuration and control options to the enabled lanes.
    b. Since the configuration is not gated and polling is enabled, the module may provide the error information from the last polling period.
    c. Error counters may also available “on demand” when the host reads the current pattern checker data but this behavior is purposely left to be vendor dependent .
2. Write 14h to the page select register. To provide better response to host, the module may return the last polled error information.
3. Write the Diagnostics Selector in byte 128 on page 14h to 02h (04h) to select lanes 1-4 for the host side (media side) or write a 03h (05h) to select host (media) lanes 5-8 (e.g. for DR8, FR8, LR8)
4. Host should read byte 138 (139) on page 14h to ensure the pattern checker has not lost lock.
5. If the host wants to reset error information, , the host shall set 13h.Byte177.Bit5 to 1. When set:
    a. Module (may also read from the data path chips and then) freezes the current error information. Since this bank’s byte 177, bit 7 is set, the module will also freeze the current error information of all enable banks with Byte 177 bit 7 set.
    b. Module copies current internal pattern checker counters into the latched counters. Again here the module will copy error information of all enable lanes and banks with Byte 177 bit 7 set to the latched error information.
6. Host may write the Diagnostics Selector in byte 128 on page 14h to 11h-15h to select and read the latched error information of all banks, by reading bytes 192-255 in Page 14h for the latched BER, error counters and total bits of the respective bank.
7. If the host wants to restart the error counter, the host shall set 13h.Byte177.Bit5 to 0. This will reset the current error information in selector 01h-05h without affecting the latched error information in 11h-15h.

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