

CP2-100MX85-1HCM

CFP2-100GBASE-SR10 850nm 100m

Features

- Supports 103.1Gb/s to 112Gb/s bit rates
- MPO 24 receptacle optical interface
- CPPI electrical interface
- Uncooled 10x10Gb/s 850nm transmitter
- 10 parallel electrical serial interface
- Applicable for 100m with OM3 MMF and 150m with OM4 MMF
- Low power consumption <4W
- Digital Diagnostic Monitor Interface
- MDIO Communication Interface
- Compliant with 100GBASE-SR10
- Operating case temperature:
- Commercial: 0 to 70 ° C



Applications

- 100GBASE-SR10 Ethernet
- 10x11.2Gb/s Multimode OTN
- 10x 10GE-SRLite Ethernet

Standards

- Compliant with IEEE 802.3ba
- Compliant with CFP2 MSA hardware specifications
- Compliant with CFP2 MSA management specifications

Description

AscentOptics' CP2-100MX85-1HCM, the 100GE SR10 CFP2 (ALT1) transceiver modules are designed for use in 100 Gigabit Ethernet links and 10x11.2G OTN client interfaces over multimode fiber. They are compliant with the CFP2 MSA and with IEEE 802.3ba 100GBASE-SR10. Digital diagnostics functions are available via the MDIO interface.

Absolute Maximum Ratings

Table 1 - Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Supply Voltage	V _{CC}	-0.5	3.6	V	
Storage Temperature	T _S	-40	85	°C	
Relative Humidity	R _H	0	85	%	
Receiver Damage Threshold	P _{Rdmg}	5			Per Lane

Recommended Operating Conditions

Table 2- Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max	Unit	Notes
Data Rate	D _R		103	112	Gb/s	
Supply Voltage	V _{CC}	3.14		3.47	V	
Operating Case Temp.	T _c	0		70	°C	

Electrical Characteristics (T_{OP} = 0 to 70°C, V_{CC} = 3.13 to 3.47 V)

Table 3- Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Data Rate Per Lane	DRPL		10.3125	11.1810	Gb/s	1
Input voltage tolerance	V _{IN}	-0.3		4	V	
Differential data input swing	V _{IN,PP}	120		1200	mVpp	2
Differential input threshold	V _{IN,TH}		50		mV	
J2 Jitter Tolerance	JT2	0.17			UI	
J9 Jitter Tolerance	JT9	0.29			UI	
Receiver						
Output voltage	V _{OUT}	-0.3		4.0	V	
Differential data output swing	V _{OUT,PP}	300		800	mVpp	3
output voltage (RMS)	PSEN2			7.5	mV	
Termination mismatch at 1 MHz	PPx			5	%	

Output rise time and fall time	Tr, Tf		28		Ps	4
J2 Jitter output	JOT2			0.42	UI	
J9 Jitter output	JOT9			0.65	UI	
Power Supply Ripple Tolerance	PRS	Per CFP MSA			mVpp	

Notes:

1. +/- 100ppm at 10.3125 Gb/s and +/-20ppm at 11.1810 Gb/s.
2. After internal AC coupling. Self-biasing 100Ω differential input.
3. AC coupled with 100Ω differential output impedance. Limiting output.
4. 20%~80%

Optical Characteristics (ToP = 0 to 70 °C, VCC = 3.13 to 3.47 V)
Table 4- Optical Characteristics

Parameter	Symbol	Min	Typical	Max.	Unit	Notes
Transmitter						
Data Rate Per Lane	D _{RPL}		10.3125	11.1810	Gb/s	1
Center wavelength	λ	840	850	860	nm	
RMS Spectral Width	Δλ			0.65	nm	
Average Power per Lane	P _{AVEP}	-8		1	dBm	
Transmit OMA per Lane	P _{OMA}	-6		3.0	dBm	2
Average launch Power of OFF	D _P			-30	dB	
Peak Power per Lane	P _P			4.0	dBm	
TDP per Lane	T _{DP}			4	dBm	
Extinction Ratio	ER	3.0			dB	
Return Loss Tolerance				12	dB	
Relative Intensity Noise	R _{IN}			-128	dB/Hz	3
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		0.23, 0.34, 0.43, 0.27, 0.35, 0.4				
Receiver						
Center wavelength	λ	840	850	860	nm	
Receiver Sensitivity per Lane	P _{SEN1}			-9.9	dBm	4
Receiver Sensitivity (OMA) per Lane	P _{SEN2}			-5.4	dBm	
Peak Power, per lane	P _{PX}			4	dBm	

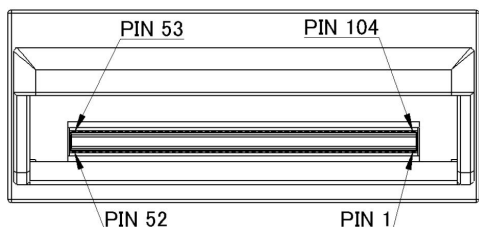
Overload,perlane	P_{AVE}	1			dBm	
Receiver Reflectance	Rrx			-12	dB	
Dispersion penalty , per lane	T_{DP}			1.9	dB	
Stressed eye J2 jitter, per Lane	J_{E2P}		0.35		UI	
Stressed eye J9 jitter, per Lane	J_{E9P}		0.47		UI	
Jitter tolerance [OMA], per lane	J_{TP}		-5.4		dBm	
LOS De-Assert	Pa	-11			dBm	
LOS Assert	Pd			-25	dBm	
LOS Hysteresis	Pd-Pa	0.5			dB	

Notes:

1. Transmitter consists of 10 lasers operating at a maximum rate of 11.1810 Gb/s each.
2. Even if TDP is <0.9dB, the OMA min must exceed this value.
3. RIN is scaled by $10 \cdot \log(10/4)$ to maintain SNR outside of transmitter.
4. Measured using DUT Tx and DUT Rx; no golden transmitters shall be used.

Pin Description

The CFP2 connector has 104 pins which are arranged in Top and Bottom rows. The pin map is shown in Picture and Table below



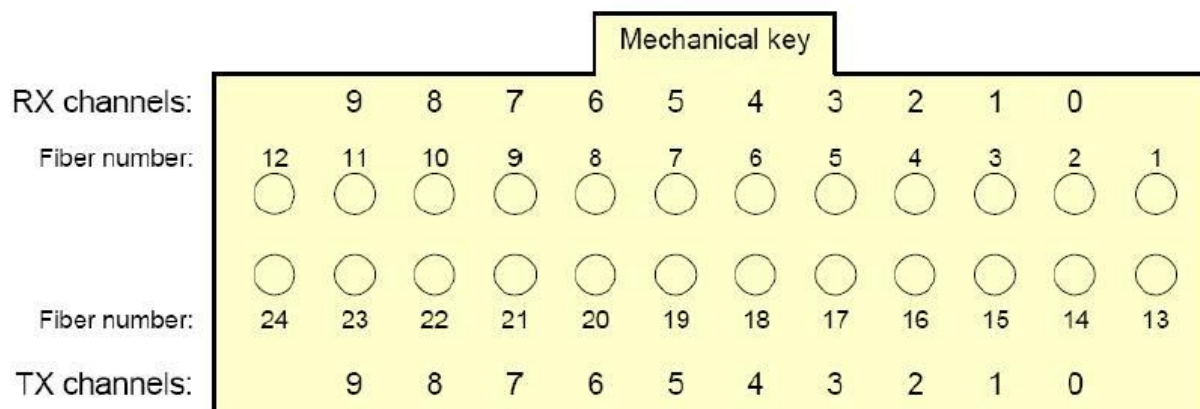
CFP2		CFP2	
Bottom Alt1		Top Alt1	
1	GND	104	GND
2	II9 _m	103	II7 _m
3	II9 _p	102	II7 _p
4	GND	101	GND
5	II8 _m	100	II6 _m
6	II8 _p	99	II6 _p
7	GND	98	GND
8	3.3V_GND	97	II5 _m
9	3.3V	96	II5 _p
10	3.3V	95	GND
11	3.3V	94	II4 _m
12	3.3V	93	II4 _p
13	3.3V_GND	92	GND
14	3.3V_GND	91	II3 _m
15	VDD_IO_A	90	II3 _p
16	VDD_IO_B	89	GND
17	FMG_CMII1	88	II2 _m
18	FMG_CMII2	87	II2 _p
19	FMG_CMII3	86	GND
20	FMG_AIRN1	85	II1 _m
21	FMG_AIRN2	84	II1 _p
22	FMG_AIRN3	83	GND
23	GND	82	II0 _m
24	II_DIS	81	II0 _p
25	II_IOS	80	GND
26	MOD_IOPWR	79	(REFCLK _m)
27	MOD_AKS	78	(REFCLK _p)
28	MOD_RST _m	77	GND
29	GLE_AIRN _m	76	II7 _m
30	GND	75	II7 _p
31	ADC	74	GND
32	ADIO	73	II6 _m
33	FMTADR0	72	II6 _p
34	FMTADR1	71	GND
35	FMTADR2	70	II5 _m
36	VDD_IO_C	69	II5 _p
37	VDD_IO_D	68	GND
38	VDD_IO_E	67	II4 _m
39	3.3V_GND	66	II4 _p
40	3.3V_GND	65	GND
41	3.3V	64	II3 _m
42	3.3V	63	II3 _p
43	3.3V	62	GND
44	3.3V	61	II2 _m
45	3.3V_GND	60	II2 _p
46	GND	59	GND
47	II9 _m	58	II1 _m
48	II9 _p	57	II1 _p
49	GND	56	GND
50	II8 _m	55	II0 _m
51	II8 _p	54	II0 _p
52	GND	53	GND

PIN#	Description	PIN#	Description
1	GND	104	GND

2	TX9n	103	TX7n
3	TX9p	102	TX7p
4	GND	101	GND
6	TX8p	99	TX6p
7	3.3V_GND	98	GND
8	3.3V_GND	97	TX5n
9	3.3V	96	TX5p
10	3.3V	95	GND
11	3.3V	94	TX4n
12	3.3V	93	TX4p
13	3.3V_GND	92	GND
14	3.3V_GND	91	TX3n
15	VND_IO_A	90	TX3p
16	VND_IO_B	89	GND
17	PRG_CNTL1	88	TX2n
18	PRG_CNTL2	87	TX2p
19	PRG_CNTL3	86	GND
20	PRG_ALARM1	85	TX1n
21	PRG_ALARM2	84	TX1p
22	PRG_ALARM3	83	GND
23	GND	82	TX0n
24	TX_DIS	81	TX0p
25	RX_LOS	80	GND
26	MOD_LOPWR	79	(REFCLKn)
27	MOD_ABS	78	(REFCLKp)
28	MOD_RSTn	77	GND
29	GLB_ALARMn	76	RX7n
30	GND	75	RX7p
31	MDC	74	GND

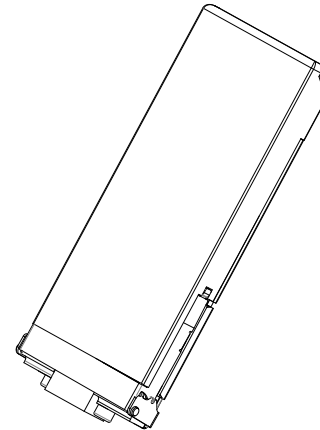
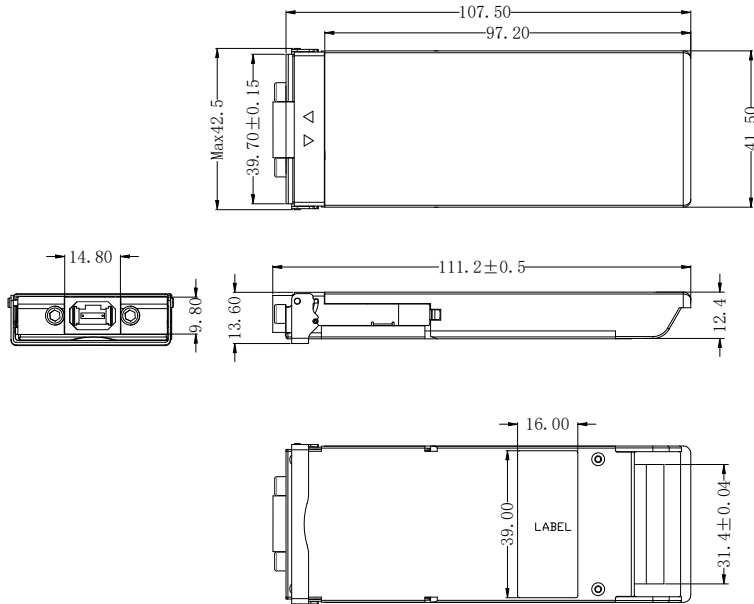
32	MDIO	73	RX6n
33	PRTADR0	72	RX6p
34	PRTADR1	71	GND
35	PRTADR2	70	RX5n
36	VND_IO_C	69	RX5p
37	VND_IO_D	68	GND
38	VND_IO_E	67	RX4n
39	3.3V_GND	66	RX4p
40	3.3V_GND	65	GND
41	3.3V	64	RX3n
42	3.3V	63	RX3p
43	3.3V	62	GND
44	3.3V	61	RX2n
45	3.3V_GND	60	RX2p
46	3.3V_GND	59	GND
47	RX9n	58	RX1n
48	RX9p	57	RX1p
49	GND	56	GND
50	RX8n	55	RX0n
51	RX8p	54	RX0p
52	GND	53	GND

Optical lane assignment (front view of MPO receptacle)



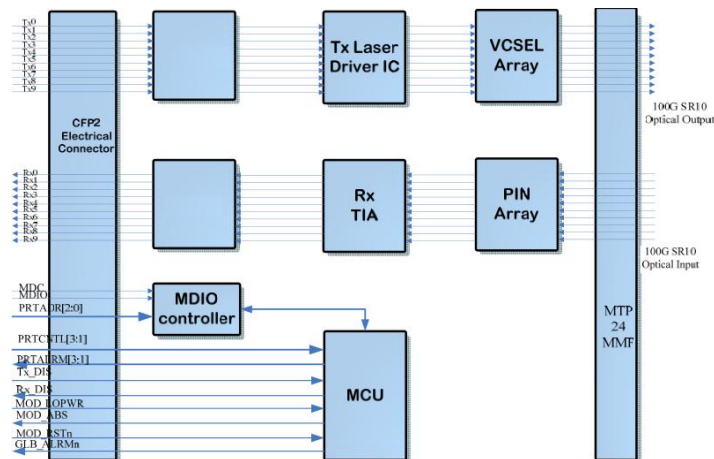
Fiber number	Channel	Electrical pin	Fibe rnumber	Channel	Electrical pin
1	Unused		13	Unused	
2	RX0	54,55	14	TX0	81,82
3	RX1	57,58	15	TX1	84,85
4	RX2	60,61	16	TX2	87,88
5	RX3	63,64	17	TX3	90,91
6	RX4	66,67	18	TX4	93,94
7	RX5	69,70	19	TX5	96,97
8	RX6	72,73	20	TX6	99,100
9	RX7	75,76	21	TX7	102,103
10	RX8	51,50	22	TX8	6,5
11	RX9	48,47	23	TX9	3,2
12	Unused		24	Unused	

Package Dimensions



Units in mm
Tolerance without indication is ±0.2mm

Functional Diagram



Ordering information

Table 5- Ordering information

Part Number	Product Description
CP2-100MX85-1HCM	CFP2 100G SR10 850nm 100m 0°C~+70°C

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