

QSP-50L231-80C

Features

- Supports 50GBASE 50GE;
- Lane bit rate 26.5625 Gb/s 50GE;
- Up to 80km transmission on SMF;
- LAN WDM EML laser and PIN receiver with SOA;
- High speed I/O electrical interface (CAUI-4);
- I2C interface with integrated Digital Diagnostic monitoring;
- QSFP28 MSA package with duplex LC connector;
- Single +3.3V power supply;
- Maximum power consumption 5.5 W;
- Operating case temperature: 0 to +70 °C;
- High Speed Electrical Interface Compliant to CAUI4;
- Compliant to SFF-8665 and SFF-8679;
- Complies with EU Directive 2015/863/EU;



Application

- 50GBASE-ZR2;

Absolute Maximum Ratings

Table 1-Absolute Maximum Ratings

| Parameter | Symbol | Min. | Typical | Max. | Unit | Notes |
|-----------------------------|-----------------|------|---------|------|------|-------|
| Storage Temperature | T _s | -40 | - | +85 | °C | |
| Supply Voltage | V _{CC} | -0.5 | - | +4.0 | V | |
| Operating Relative Humidity | RH | - | - | +85 | % | |

Recommended Operating Conditions

Table 2-Recommended Operating Conditions

| Parameter | Symbol | Min. | Typical | Max. | Unit | Notes |
|----------------------------|-----------------|------|---------|------|------|-------|
| Operating Case Temperature | TC | 0 | - | +70 | °C | |
| Power Supply Voltage | V _{CC} | 3.13 | 3.3 | 3.47 | V | |
| Power Supply Current | I _{CC} | - | - | 1.66 | A | |

| | | | | | | |
|---------------------------|--------|---|---------|-----|------|----------|
| Maximum Power Dissipation | PD | - | - | 5.5 | W | |
| Aggregate Bit Rate | BRAVE | - | 53.125 | - | Gb/s | |
| Lane Bit Rate | BRLANE | - | 26.5625 | - | Gb/s | |
| Transmission Distance | TD | | - | 80 | km | Over SMF |

Optical Characteristics

Table 3-Optical Characteristics

| Transmitter | | | | | | |
|--|---|---------|---------|-------------|-------|-------|
| Parameter | Symbol | Min. | Typical | Max. | Unit | Notes |
| Center Wavelength Lane 1 | λ_0 | 1303.54 | 1304.58 | 1305.6 3 | nm | |
| Center Wavelength Lane 2 | λ_1 | 1308.09 | 1309.14 | 1310.1 9 | nm | |
| Total Launch Power | PALL | 5 | - | 9.5 | dBm | 1 |
| Average Launch Power per Lane | PTX_LANE | 2 | - | 6.5 | dBm | 1 |
| OMA per Lane | OMA | 3.6 | - | 8.1 | dBm | 1 |
| Difference in launch power between lanes | PTX_Delta_LANE | - | - | 3.6 | dB | |
| Average Output Power (Laser Turn off) | P0UT-OFF | - | - | -30 | dBm | |
| Side Mode Suppression Ratio | SMSR | 30 | - | - | dB | |
| Extinction Ratio | ER | 8 | - | - | dB | |
| RIN_OMA | RIN | - | - | -130 | dB/Hz | |
| Transmitter and Dispersion Penalty | TDP | - | - | 2.5 | dB | 2 |
| Transmitter reflectance | Tref | - | - | -12 | dB | |
| Optical Return Loss Tolerance | ORLT | - | - | 20 | dB | |
| Optical Eye Mask | Compliant with IEEE 802.3bm {0.25, 0.4, 0.45, 0.25, 0.28, 0.4} | | | | | 2 |
| Receiver | | | | | | |
| Center Wavelength Lane 0 | λ_0 | 1303.54 | 1304.58 | 1305.6 3 | nm | |
| Center Wavelength Lane 1 | λ_1 | 1308.09 | 1309.14 | 1310.1 9 | nm | |
| Damage threshold | Pdamage | 5.5 | - | - | dBm | |
| Average Rx Power per Lane | PRx_LANE | -29 | - | 4.5 | dBm | 3 |
| OMA Sensitivity per Lane | POMA_LANE | - | - | -26.4 | dBm | 3 |
| Los Assert | LosA | -40 | - | - | dBm | |
| Los De-assert | LosDA | - | - | -29 | dBm | |
| Los Hysteresis | LosH | 0.5 | - | - | dB | |

Notes:

1. The optical power is launched into SMF.
2. Measured with a PRBS $2^{31}-1$ test pattern @26.5625 Gb/s, Hit ratio $\leq 2E-4$.
3. Measured with a PRBS $2^{31}-1$ test pattern @26.5625 Gb/s, BER $\leq 2E-4$.

Electrical Characteristics

Table 4-Electrical Characteristics

| Transmitter (Module Input) | | | | | | |
|--|----------|---|---------|---------|------|-------|
| Parameter | Symbol | Min. | Typical | Max. | Unit | Notes |
| Differential Data Input Amplitude | VIN,P-P | 85 | - | 900 | mVpp | |
| Differential Termination Mismatch | | - | - | 10 | % | |
| Differential input return loss(min) | RLd(f) | 9.5 - 0.37f, 0.01 ≤ f < 8 4.75 - 7.4log10(f/14), 8 ≤ f < 19 | | | dB | |
| Differential to common mode input return loss (min) | RLdc(f) | 22-20(f/25.78), 0.01 ≤ f < 12.89 15-6(f/25.78), 12.89 ≤ f < 19 | | | dB | |
| LPMODE, Reset and ModSelL, V in low | VIL | -0.3 | - | 0.8 | V | |
| LPMODE, Reset and ModSelL, V in high | VIH | 2.0 | - | VCC+0.3 | V | |
| Receiver (Module Output) | | | | | | |
| Differential Data Output Amplitude | VOUT,P-P | 200 | - | 900 | mVpp | |
| Differential Termination Mismatch (1MHZ) | | - | - | 10 | % | |
| Transition time, 20% to 80% | Tr Tf | 12 | - | - | ps | |
| Differential output return loss (min) | RLd(f) | 9.5 - 0.37f, 0.01 ≤ f < 8 4.75 - 7.4log10(f/14), 8 ≤ f < 19 | | | dB | |
| Common to differential mode conversion return loss (min) | RLdc(f) | 22-20(f/25.78), 0.01 ≤ f < 12.89 15-6(f/25.78), 12.89 ≤ f < 19 | | | dB | |
| ModPrsL and IntL, V out low | VOL | 0 | - | 0.4 | V | |
| ModPrsL and IntL, V out high | VOH | VCC-0.5 | - | VCC+0.3 | V | |

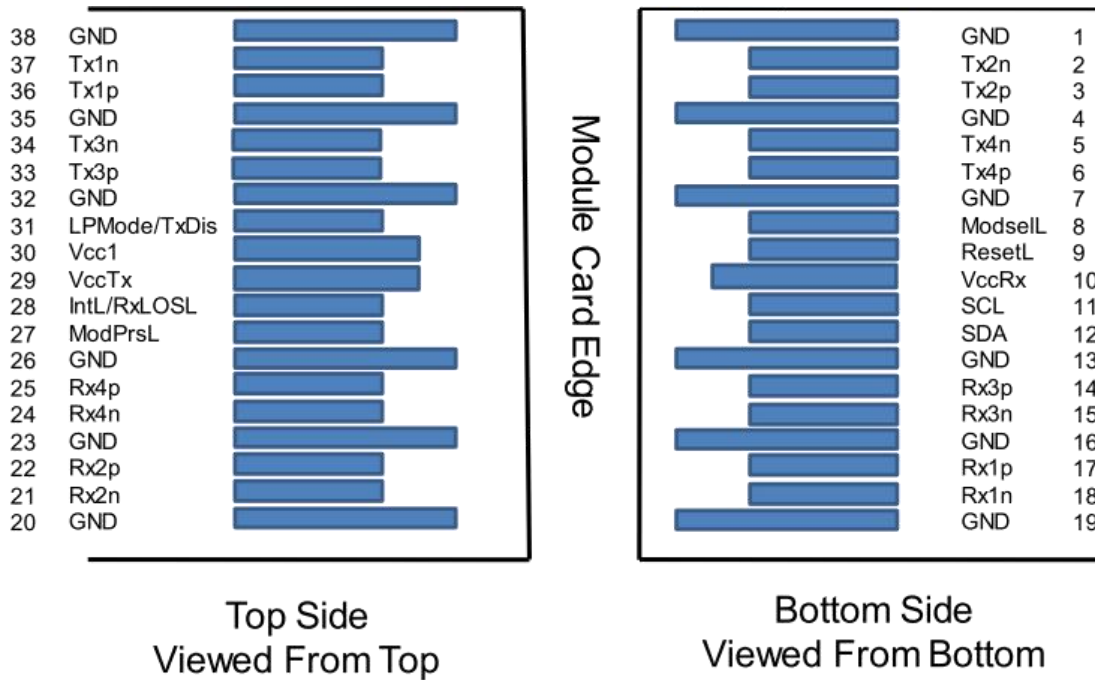
Digital Diagnostics

Table 5-Digital Diagnostics

| Parameter | Range | Accuracy | Unit | Calibration |
|--------------------------|------------|----------|------|-------------|
| Temperature | 0 to 70 | ±3 | °C | Internal |
| Voltage | 0 to VCC | 0.1 | V | Internal |
| Tx Bias Current Per Lane | 0 to 100 | 10% | mA | Internal |
| Tx Output Power Per Lane | 2.0 to 6.5 | ±3 | dBm | Internal |
| Rx Power (Each Lane) | -28 to 4.5 | ±3 | dBm | Internal |

Pin Assignment

Pin Diagram



Pin Descriptions

Table 6- Pin Descriptions

| PIN | Logic | Symbol | Description | PlugSeq. | Notes |
|-----|-------------|---------|--------------------------------------|----------|-------|
| 1 | | GND | Ground | 1 | 1 |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input | 3 | |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data output | 3 | |
| 4 | | GND | Ground | 1 | 1 |
| 5 | CML-I | Tx4n | NC | 3 | |
| 6 | CML-I | Tx4p | NC | 3 | |
| 7 | | GND | Ground | 1 | 1 |
| 8 | LVTLL-I | ModSelL | Module Select | 3 | |
| 9 | LVTLL-I | ResetL | Module Reset | 3 | |
| 10 | | VccRx | + 3.3V Power Supply Receiver | 2 | 2 |
| 11 | LVC MOS-I/O | SCL | 2-Wire Serial Interface Clock | 3 | |
| 12 | LVC MOS-I/O | SDA | 2-Wire Serial Interface Data | 3 | |
| 13 | | GND | Ground | 1 | |
| 14 | CML-O | Rx3p | NC | 3 | |
| 15 | CML-O | Rx3n | NC | 3 | |
| 16 | | GND | Ground | 1 | 1 |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output | 3 | |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output | 3 | |

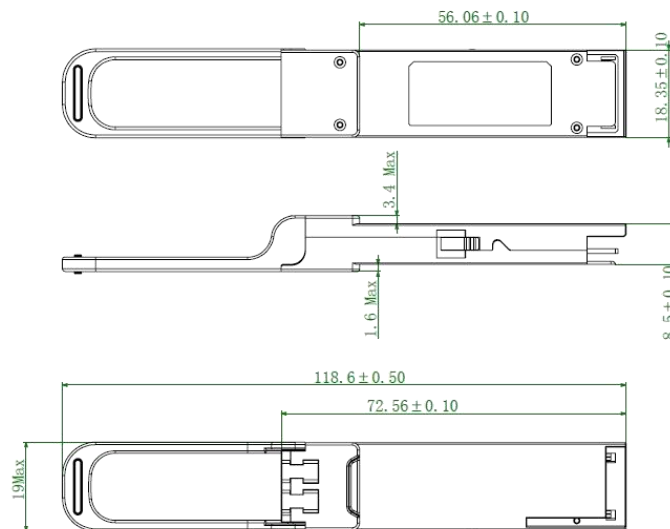
| | | | | | |
|----|----------|--------------|-------------------------------------|---|---|
| 19 | | GND | Ground | 1 | 1 |
| 20 | | GND | Ground | 1 | 1 |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output | 3 | |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output | 3 | |
| 23 | | GND | Ground | 1 | 1 |
| 24 | CML-O | Rx4n | NC | 3 | |
| 25 | CML-O | Rx4p | NC | 3 | |
| 26 | | GND | Ground | 1 | 1 |
| 27 | LVTTTL-O | ModPrsL | Module Present | 3 | |
| 28 | LVTTTL-O | IntL/Rx_LOS | Interrupt/Rx_LOS | 3 | |
| 29 | | VccTx | +3.3 V Power Supply transmitter | 2 | 2 |
| 30 | | Vcc1 | +3.3 V Power Supply | 2 | 2 |
| 31 | LVTTTL-I | LPMode/TxDIS | Low Power Mode/Tx_Disable | 3 | |
| 32 | | GND | Ground | 1 | 1 |
| 33 | CML-I | Tx3p | NC | 3 | |
| 34 | CML-I | Tx3n | NC | 3 | |
| 35 | | GND | Ground | 1 | 1 |
| 36 | CML-I | Tx1p | Transmitter Non-Inverted Data Input | 3 | |
| 37 | CML-I | Tx1n | Transmitter Inverted Data Output | 3 | |
| 38 | | GND | Ground | 1 | 1 |

Note :

1.GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2.Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in MSA. The connector pins are each rated for a maximum current of 1000 mA.

Mechanical Dimension



Ordering information

Table 7- Ordering information

| Part Number. | Description |
|----------------|--|
| QSP-50L231-80C | 53.125Gbps, LWDM, SMF, 80km, LC, 0~70C, with DDM |

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E-mail: sales@ascentoptics.com

Web : <http://www.ascentoptics.com>